phyFLEX®-AM335x

Hardware Manual

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List of Figures

List of Tables

Conventions, Abbreviations and Acronyms

This hardware manual describes the PFL-A-03 System on Module in the following referred to as phyFLEX®-AM335x. The manual specifies the phyFLEX®-AM335x's design and function. Precise specifications for the Texas Instruments AM335x microcontrollers can be found in the enclosed microcontroller Data Sheet/User's Manual.

Note:
We refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products. Please read the paragraph "**Product Change Management and information in this manual on parts populated on the SOM"** within the *Preface*.

Note:
The BSP delivered with the phyFLEX®-AM335x usually includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore programming close to hardware at register level is not necessary in most cases. For this reason, this manual contains no detailed description of the controller's registers, or information relevant for software development. Please refer to the *AM335x Reference Manual*, if such information is needed to connect customer designed applications.

Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n", "/", or "#"character (e.g.: nRD, /RD, or #RD), or that have a dash on top of the signal name (e.g.: $\overline{\text{RD}}$) are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 MSB of the address byte. The correct value of the LSB which depends on the desired command (read (1), or write (0)) must be added to get the complete address byte. E.g. given address in this manual 0x41 => complete address byte = 0x83 to read from the device and 0x82 to write to the device
- Tables which describe jumper settings show the default position in **bold, blue text.**
- Text in *blue italic* indicates a hyperlink within, or external to the document. Click these links to quickly jump to the applicable URL, part, chapter, table, or figure.
- References made to the phyFLEX-Connector always refer to the high-density samtec connector on the undersides of the phyFLEX-AM335x System on Module.

Types of Signals

Different types of signals are brought out at the phyFLEX-Connector. The following table lists the abbreviations used to specify the type of a signal.

Signal Type	Description	Abbr.
Power	Supply voltage input	PWR_I
Ref-Voltage	Reference voltage output	REF_O
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
IPU	Digital input with pull-up, must only be connected to GND. (jumper or open-collector output)	IPU
OC-Bidir PU	Open collector input/output with pull up	OC-BI
OC-Output	Open collector output without pull up, requires an external pull up	OC
5V Input PD	5 V tolerant input with pull down	5V_PD
LVDS Input	Differential line pairs 100 Ohm LVDS level input	LVDS_I
LVDS Output	Differential line pairs 100 Ohm LVDS level output	LVDS_O
LVDS IO	Differential line pairs 100 Ohm LVDS level bidirectional input/output	LVDS_I/O
TMDS Output	Differential line pairs 100 Ohm TMDS level output	TMDS_O
USB IO	Differential line pairs 90 Ohm USB level bidirectional input/output	USB_I/O
ETHERNET Input	Differential line pairs 100 Ohm Ethernet level input	ETH_I
ETHERNET Output	Differential line pairs 100 Ohm Ethernet level onput	ETH_O
ETHERNET IO	Differential line pairs 100 Ohm Ethernet level bidirectional input/output	ETH_I/O
PCIe Input	Differential line pairs 100 Ohm PCIe level input	PCIe_I
PCIe Output	Differential line pairs 100 Ohm PCIe level output	PCIe_O
MLB Output	Differential line pairs 100 Ohm Media local bus output	MLB_O
MLB IO	Differential line pairs 100 Ohm Media local bus bidirectional input/output	MLB_I/O
MIPI CSI-2 Input	Differential line pairs 100 Ohm MIPI CSI-2 level input	CSI-2_I

Table 1: Signal Types used in this Manual

Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Windows, or Linux) preinstalled on the module and Development Tools).
CB	Carrier Board; used in reference to the phyFLEX Development Kit Carrier Board.
DFF	D flip-flop.
EMB	External memory bus.
EMI	Electromagnetic Interference.
GPI	General purpose input.
GPIO	General purpose input and output.
GPO	General purpose output.
IRAM	Internal RAM; the internal static RAM on the Texas Instruments AM335x microcontroller.
J	Solder jumper; these types of jumpers require solder equipment to remove and place.
JP	Solderless jumper; these types of jumpers can be removed and placed by hand with no special tools.
PCB	Printed circuit board.
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Extension Board
PMIC	Power management IC
PoE	Power over Ethernet
POR	Power-on reset
RTC	Real-time clock.
SMT	Surface mount technology.
SOM	System on Module; used in reference to the PFL-A-03 /phyFLEX®-AM335x module
Sx	User button Sx (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the carrier board.
Sx_y	Switch y of DIP-Switch Sx; used in reference to the DIP-Switch on the carrier board.

Table 2: Abbreviations and Acronyms used in this Manual

Preface

As a member of PHYTEC's new phyFLEX® product family the phyFLEX-AM335x is one of a series of PHYTEC System on Modules (SOMs) that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports a variety of 8-/16- and 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional phyFLEX® OEM modules, which can be embedded directly into the user's peripheral hardware design.

Implementation of an OEM-able SOM subassembly as the "core" of your embedded design allows you to focus on hardware peripherals and firmware without expending resources to "re-invent" microcontroller circuitry. Furthermore, much of the value of the phyFLEX® module lies in its layout and test.

PHYTEC's new phyFLEX® product family consists of a series of extremely compact embedded control engines featuring various processing performance classes while using the newly developed phyFLEX® embedded bus standard. The standardized connector footprint and pin assignment of the phyFLEX® bus makes this new SOM generation extremely scalable and flexible. This also allows to use the same carrier board to create different applications depending on the required processing power. With this new SOM concept it is possible to design entire embedded product families around vastly different processor performances while optimizing overall system cost. In addition, future advances in processor technology are already considered with this new embedded bus standard making product upgrades very easy. Another major advantage is the forgone risk of potential system hardware redesign steps caused by processor or other critical component discontinuation. Just use one of PHYTEC's other phyFLEX® SOMs thereby ensuring an extended product life cycle of your embedded application.

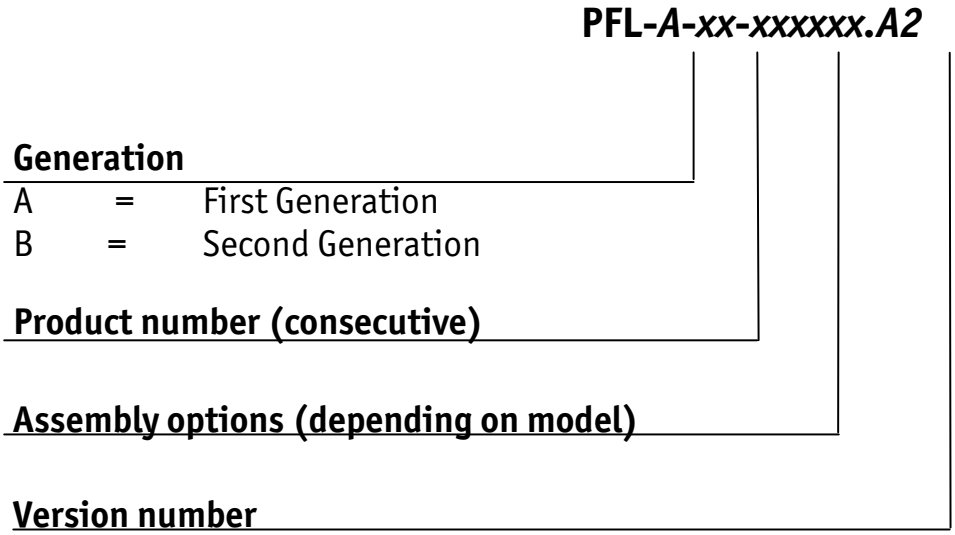
Production-ready Board Support Packages (BSPs) and Design Services for our hardware will further reduce your development time and risk and allow you to focus on your product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution you will be able to bring your new ideas to market in the most timely and cost-efficient manner.

For more information go to:

http://www.phytec.de/de/leistungen/entwicklungsunterstuetzung.html or
www.phytec.eu/europe/oem-integration/evaluation-start-up.html

Ordering Information

The part numbering of the phyFLEX has the following structure:



In order to receive product specific information on changes and updates in the best way also in the future, we recommend to register at

http://www.phytec.de/de/support/registrierung.html or
http://www.phytec.eu/europe/support/registration.html

For technical support and additional information concerning your product, please visit the support section of our web site which provides product specific information, such as errata sheets, application notes, FAQs, etc.

http://www.phytec.de/de/support/faq/faq-phyFLEX-AM335x.html or
http://www.phytec.eu/europe/support/faq/faq-phyFLEX-AM335x.html

Declaration of Electro Magnetic Conformity of the PHYTEC phyFLEX®-AM335x

PHYTEC System on Module (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution!
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

Product Change Management and information in this manual on parts populated on the SOM

When buying a PHYTEC SOM, you will, in addition to our HW and SW offerings, receive a free obsolescence maintenance service for the HW we provide.

Our PCM (Product Change Management) Team of developers, is continuously processing, all incoming PCN's (Product Change Notifications) from vendors and distributors concerning parts which are being used in our products.

Possible impacts to the functionality of our products, due to changes of functionality or obsolesce of a certain part, are being evaluated in order to take the right masseurs in purchasing or within our HW/SW design.

Our general philosophy here is: **We never discontinue a product as long as there is demand for it.**

Therefore we have established a set of methods to fulfill our philosophy:

Avoiding strategies

- Avoid changes by evaluating longlivety of parts during design in phase.
- Ensure availability of equivalent second source parts.
- Stay in close contact with part vendors to be aware of roadmap strategies.

Change management in rare event of an obsolete and non replaceable part

- Ensure long term availability by stocking parts through last time buy management according to product forecasts.
- Offer long term frame contract to customers.

Change management in case of functional changes

- Avoid impacts on product functionality by choosing equivalent replacement parts.
- Avoid impacts on product functionality by compensating changes through HW redesign or backward compatible SW maintenance.
- Provide early change notifications concerning functional relevant changes of our products.

Therefore we refrain from providing detailed part specific information within this manual, which can be subject to continuous changes, due to part maintenance for our products.

In order to receive reliable, up to date and detailed information concerning parts used for our product, please contact our support team through the given contact information within this manual.

1 Introduction

The phyFLEX-AM335x belongs to PHYTEC's phyFLEX System on Module family. The phyFLEX SOMs represent the continuous development of PHYTEC System on Module technology. Like its mini-, micro- and nanoMODUL predecessors, the phyFLEX boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

PHYTEC's phyFLEX family introduces the newly developed phyFLEX embedded bus standard. Apart from processor performance, a large number of embedded solutions require a corresponding number of standard interfaces. Among these process interfaces are for example Ethernet, USB, UART, SPI, I^2C, PCIe, audio, and display connectivity. The phyFLEX bus exactly meets this requirement with the phyFLEX-fix connector. As well the location of the commonly used interfaces as the mechanical specifications are clearly defined. Beside this, the phyFLEX concept also considers, that different controllers have many different interfaces. To take this into account, the phyFLEX concept allows two more connectors: the phyFLEX-optional connector, which has optional, but defined interfaces at fixed positions (e.g. SATA, CAN, camera) and the phyFLEX-flex connector, which has only fixed Ground signals. All other signals of the phyFLEX-flex connector are module specific. All interface signals of PHYTEC's new phyFLEX bus are available on up to three, high-density pitch (0.5 mm) connectors, allowing the phyFLEXs to be plugged like a "big chip" into a target application.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments approximately 20 % of all pin header connectors on the phyFLEX bus are dedicated to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyFLEX boards even in high noise environments.

phyFLEX boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled microvias are used on the boards, providing phyFLEX users with access to this cutting edge miniaturization technology for integration into their own design.

The phyFLEX-AM335x is a subminiature (50 mm x 50 mm) insert-ready System on Module populated with the Texas Instruments AM335x microcontroller. Its universal design enables its insertion in a wide range of embedded applications.

Precise specifications for the controller populating the board can be found in the applicable controller reference manual or datasheet. The descriptions in this manual are based on the Texas Instruments AM335x. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyFLEX-AM335x.

The phyFLEX-AM335x offers the following features:

- Subminiature System on Module (50 mm x 50 mm) achieved through modern SMD technology
- Populated with the Texas Instruments AM335x microcontroller (BGA324 packaging)
- Max. 1 GHz core clock frequency
- Boot from different memory devices (NAND Flash (standard))
- phyFLEX bus. Commonly used interfaces such as Ethernet, USB, UART, SPI, I^2C, audio, CAN, and display connectivity (LVDS) are available at up to two high-density (0.5 mm) samtec connectors, enabling the phyFLEX-AM335x to be plugged like a "big chip" into target application
- Single supply voltage of 5 V
- All controller required supplies generated on board
- Improved interference safety achieved through multi-layer PCB technology and dedicated ground pins
- 128 MB (up to 512 MB) DDR3 SDRAM
- 128 MB (up to 1 GB) on-board NAND Flash
- 8 MB on-board serial Flash (bootable)
- 4 kB I^2C EEPROM
- Two Serial interface (one with 4 lines (TTL) allowing simple hardware handshake)
- High-Speed USB OTG transceiver
- High-Speed USB HOST transceiver
- 10/100/1000 Mbit Ethernet interface (ETH0)
- 10/100 Mbit Ethernet interface (ETH1)
- I^2C interface
- Two SPI interfaces
- I^2S Interface
- CAN interface
- 4 Channel LVDS (24 Bit) LCD-Interface
- One SD/MMC card interfaces
- Support of standard 20 pin debug interface through JTAG connector
- Eleven dedicated GPIO/IRQ ports at the phyFLEX-fix connector
- Power Management IC (PMIC)
- Control Management IC (CMIC)
- Optional Environment Management IC (EMIC) to monitor voltage, current and temperature, and for fan control
- One Wake Up input
- Industrial temperature range (-40 °C to +85 °C)

1.1 Block Diagram

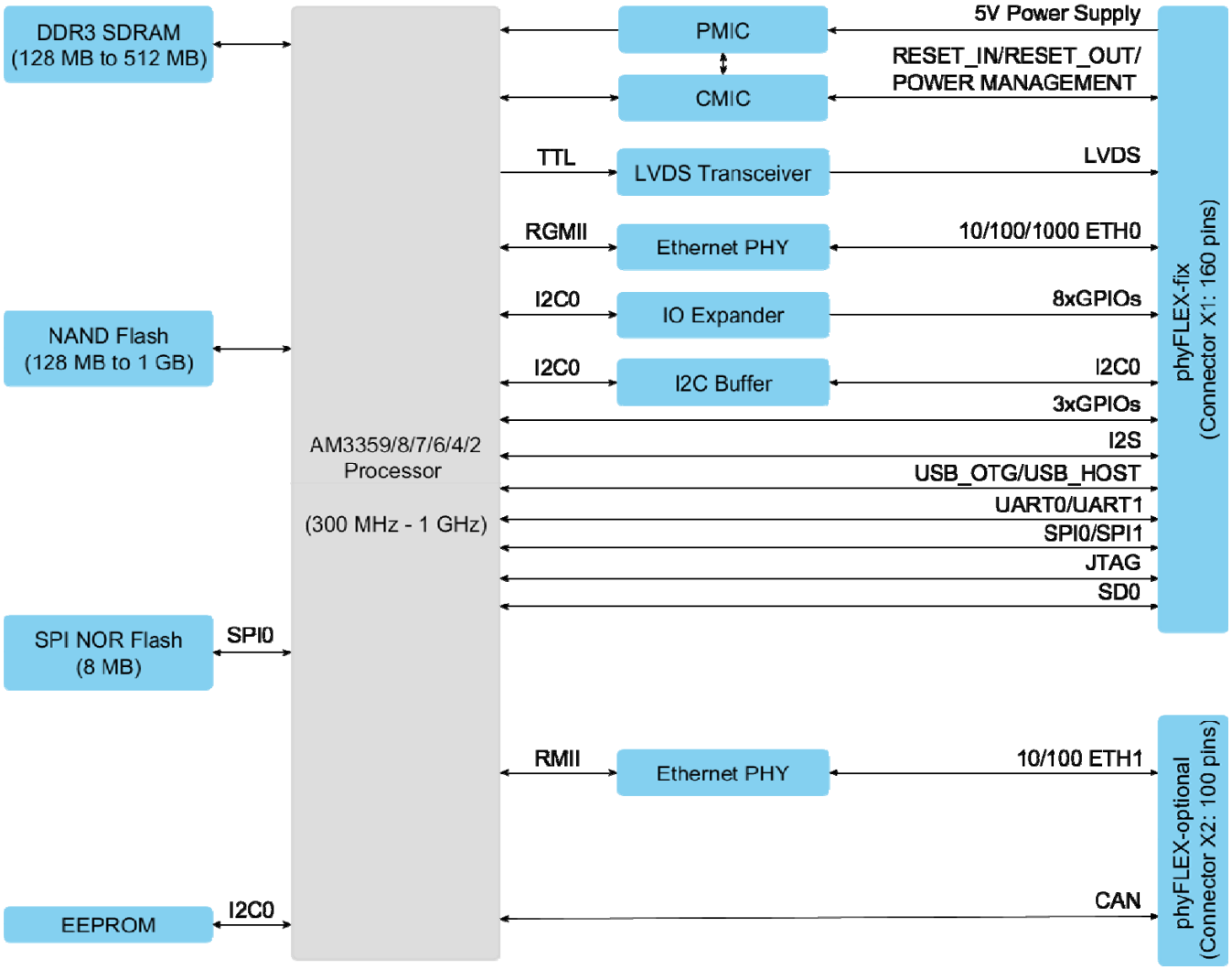


Figure 1: Block Diagram of the phyFLEX-AM335x

1.2 phyFLEX-AM335x Component Placement

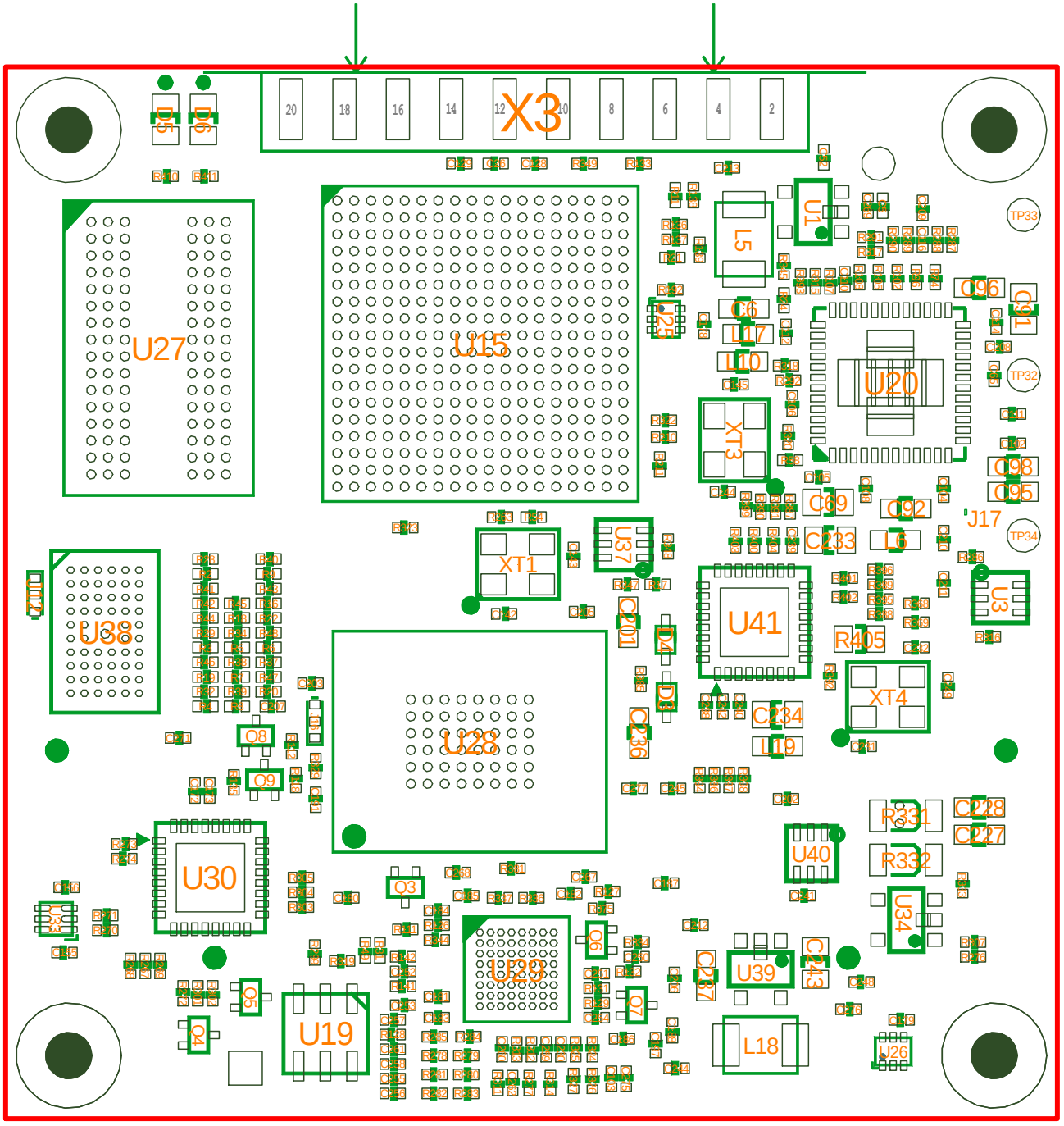


Figure 2: phyFLEX-AM335x Component Placement (top view)

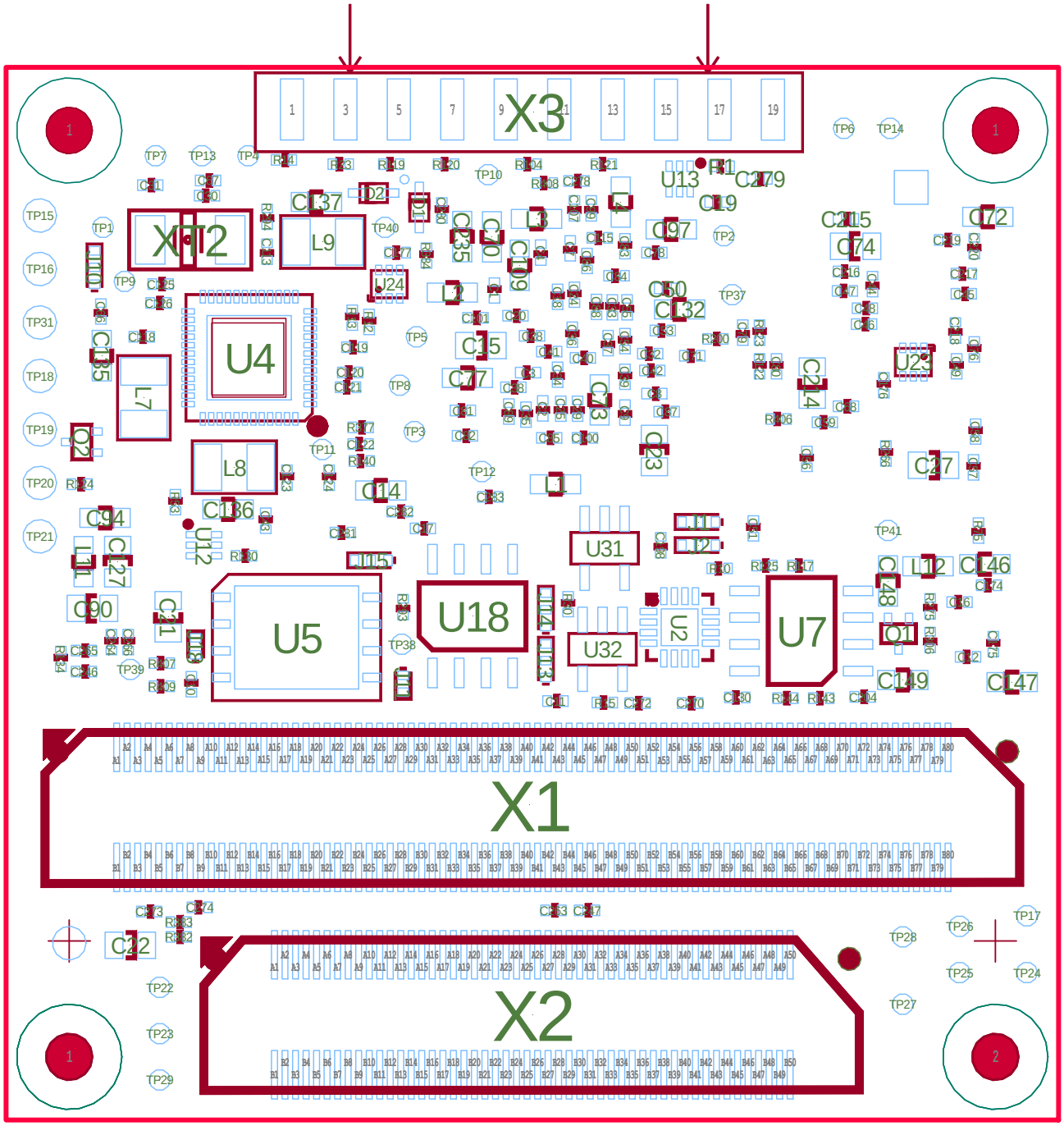


Figure 3: phyFLEX-AM335x Component Placement (bottom view)

1.3 Minimum Requirements to operate the phyFLEX-AM335x

Basic operation of the phyFLEX-AM335x only requires supply of a +5 V input voltage with 2 A load and the corresponding GND connection.

These supply pins are located at the phyFLEX-Connector X1:

VDD_5V_IN_R: X1 A1, A2, A3, B1, B2, B3

Connect all +5 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 A4, A10, A16, B4, B7, B13

Please refer to *section 2* for information on additional GND Pins located at the phyFLEX-Connector X1.

Caution!
We recommend connecting all available +5 V input pins to the power supply system on a custom carrier board housing the phyFLEX-AM335x and at least the matching number of GND pins neighboring the +5 V pins.

In addition, proper implementation of the phyFLEX-AM335x module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to *section 4* for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

All phyFLEX bus signals extend to up to three surface mount technology (SMT) connectors (0.5 mm) (referred to as phyFLEX-Connector). The phyFLEX-AM335x is equipped with two connectors (phyFLEX-fix and phyFLEX-optional) as *Figure 4* indicates. This allows the phyFLEX-AM335x to be plugged into any target application like a "big chip". As well the location of the commonly used interfaces as the mechanical specifications of the connectors are clearly defined.

The first connector X1 is called phyFLEX-fix connector. All phyFLEX SOMs support all interfaces specified for this connector at the same locations. The second connector X2, called phyFLEX-optional connector, has optional, but defined interfaces at fixed positions (e.g. SATA[1], CAN[1], camera[1]). phyFLEX SOMs can, but do not have to support the interfaces at the phyFLEX-optional connector. The third connector, phyFLEX-flex connector X3 (not available on the phyFLEX-AM335x), has only fixed Ground signals. All other signals of the phyFLEX-flex connector are module specific and depend on the features of the controller populating the SOM.

The numbering scheme for the phyFLEX-Connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number with prefixed Connector Reference (X1=phyFLEX-fix, X2=phyFLEX-optional, X3=phyFLEX-flex). Pin X1A1, for example, is always located in the upper left hand corner of the matrix of connector X1. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (refer to *Figure 4*).

The numbered matrix can be aligned with the phyFLEX-AM335x (viewed from above; phyFLEX-Connector pointing down) or with the socket of the corresponding phyFLEX Carrier Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin X1A1) is thus covered with the corner of the phyFLEX-AM335x. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyFLEX-Connector as well as the mating connector on the phyFLEX Carrier Board or target hardware, thereby considerably reducing the risk of pin identification errors.

[1]: if supported by the SOM

The following figure illustrates the numbered matrix system. It shows a phyFLEX-AM335x with two SMT phyFLEX-Connectors on its underside (defined as dotted lines) mounted on a carrier board. In order to facilitate understanding of the pin assignment scheme, the diagram presents a cross-view of the phyFLEX-AM335x module showing the phyFLEX-Connector mounted on the underside of the module's PCB.

Table 3 to *6* provide an overview of the pinout of the different phyFLEX-Connectors X1, X2, and X3 with signal names and descriptions specific to the phyFLEX-AM335x. It also provides the appropriate voltage domain, signal type (ST) and a functional grouping of the signals. The signal type includes also information about the signal[1]. A description of the signal types can be found in *Table 1*.

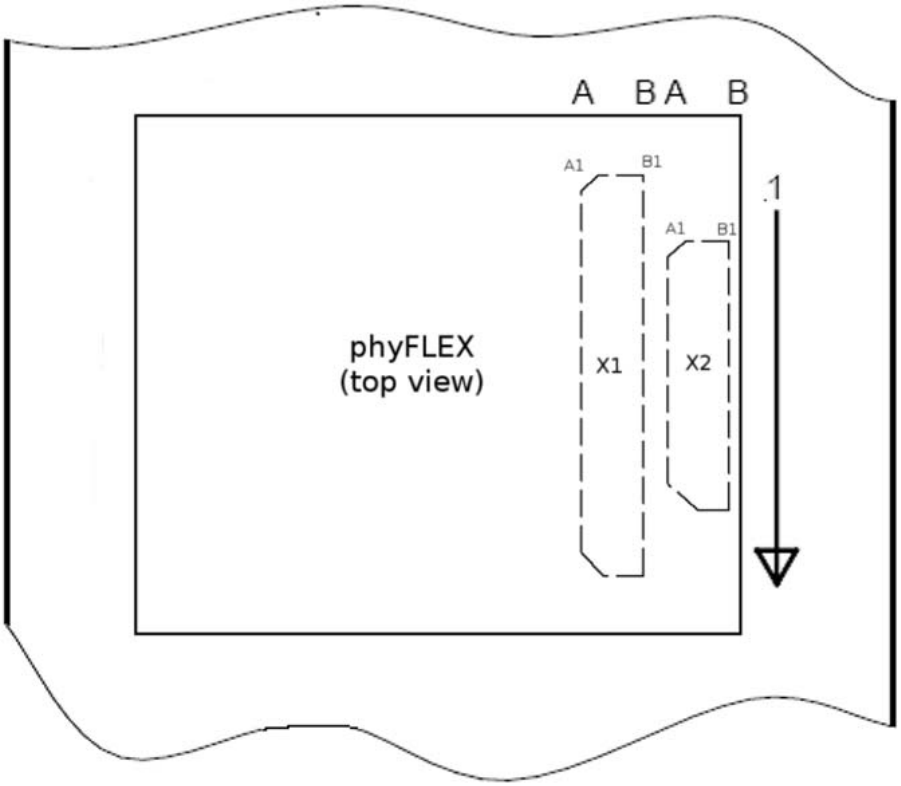


Figure 4: Pinout of the phyFLEX-Connector (top view)

The Texas Instruments AM335x is a multi-voltage operated microcontroller and as such special attention should be paid to the interface voltage levels to avoid unintentional damage to the microcontroller and other on-board components. Please refer to the *Texas Instruments AM335x Reference Manual* for details on the functions and features of controller signals and port pins.

Note: Signals on the phyFLEX-fix (X1) and phyFLEX-optional (X2) connectors have fixed positions equal for all phyFLEX SOMs. Furthermore all phyFLEX SOMs support all interfaces specified for the phyFLEX-fix connector (X1). As opposed to this, the phyFLEX-optional connector (X2) has optional, but defined interfaces at fixed positions (e.g. ETH1, CAN). Other phyFLEX SOMs might have more, or less interfaces.

[1]: The specified direction indicated refers to the standard phyFLEX use of the pin.

Pin #	Signal	ST	Voltage domain	Description
X1A1	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A2	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A3	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1A4	GND	-	-	Ground 0 V
X1A5	X_nJTAG_TRSTB	I	VMMC_3P3V	JTAG reset input (low active)
X1A6	X_JTAG_TDI	I	VMMC_3P3V	JTAG TDI
X1A7	X_JTAG_TMS	I	VMMC_3P3V	JTAG TMS
X1A8	X_JTAG_TDO	O	VMMC_3P3V	JTAG TDO
X1A9	X_JTAG_TCK	I	VMMC_3P3V	JTAG clock input
X1A10	GND	-	-	Ground 0 V
X1A11	X_JTAG_TCK	I	VMMC_3P3V	JTAG RTCLK (connected to JTAG clock input via 0 Ohm resistor)
X1A12	X_UART1_TXD	O	VMMC_3P3V	UART1 serial transmit signal
X1A13	X_UART1_RXD	I	VMMC_3P3V	UART1 serial data receive signal
X1A14	X_UART1_RTS	O	VMMC_3P3V	UART1 request to send
X1A15	X_UART1_CTS	I	VMMC_3P3V	UART1 clear to send
X1A16	GND	-	-	Ground 0 V
X1A17	reference-voltage	REF_O	VMMC_3P3V	UART1 reference voltage
X1A18	X_UART0_TXD	O	VMMC_3P3V	UART0 serial transmit signal
X1A19	reference-voltage	REF_O	VMMC_3P3V	UART0 reference voltage
X1A20	X_UART0_RXD	I	VMMC_3P3V	UART0 serial data receive signal
X1A21	X_SPI0_MOSI	O	VMMC_3P3V	SPI0 master output/slave input
X1A22	GND	-	-	Ground 0 V
X1A23	X_SPI0_MISO	I	VMMC_3P3V	SPI0 master input/slave output
X1A24	X_SPI0_CSBOOT	O	VMMC_3P3V	SPI0 Chip Select BOOT
X1A25	X_SPI0_CS0	O	VMMC_3P3V	SPI0 Chip Select 0
X1A26	X_SPI0_CS1	O	VMMC_3P3V	SPI0 Chip Select 1
X1A27	reference-voltage	REF_O	VMMC_3P3V	SPI0 reference voltage
X1A28	GND	-	-	Ground 0 V
X1A29	X_SPI0_CLK	O	VMMC_3P3V	SPI0 clock signal
X1A30	X_SPI1_CS0	O	VMMC_3P3V	SPI1 chip select 0
X1A31	X_SPI1_MOSI	O	VMMC_3P3V	SPI1 master output/slave input

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A

Pin #	Signal	ST	Voltage domain	Description
X1A32	X_SPI1_MISO	I	VMMC_3P3V	SPI1 master input/slave output
X1A33	reference-voltage	REF_O	VMMC_3P3V	SPI1 reference voltage
X1A34	GND	-	-	Ground 0 V
X1A35	X_SPI1_CLK	O	VMMC_3P3V	SPI1 clock signal
X1A36	X_SPI1_CS1	O	VMMC_3P3V	SPI1 chip select 1
X1A37	X_nUSB0_VBUSEN	O	VMMC_3P3V	USB0 VBUS enable (active low)
X1A38	X_USB0_VBUS	PWR_I	5V	USB0 VBUS input
X1A39	X_nUSB0_OC	IPU	VMMC_3P3V	USB0 overcurrent input
X1A40	GND	-	-	Ground 0 V
X1A41	reference-voltage	REF_O	VMMC_3P3V	USB0 reference voltage
X1A42	X_USB0_CHGDET	O	VMMC_3P3V	USB0 charger detection
X1A43	X_nUSB1_VBUSEN	O	VMMC_3P3V	USB1 VBUS enable (active low)
X1A44	X_USB1_VBUS	PWR_I	5V	USB1 VBUS input
X1A45	X_nUSB1_OC	IPU	VMMC_3P3V	USB1 overcurrent input
X1A46	GND	-	-	Ground 0 V
X1A47	reference-voltage	REF_O	VMMC_3P3V	USB1 reference voltage
X1A48	X_I2S0_CLK	O	VMMC_3P3V	I^2S receive clock
X1A49	X_I2S0_FRM	O	VMMC_3P3V	I^2S receive frame
X1A50	X_I2S0_ADC	I	VMMC_3P3V	I^2S receive data
X1A51	reference-voltage	REF_O	VMMC_3P3V	I^2S reference voltage
X1A52	GND	-	-	Ground 0 V
X1A53	X_I2S0_DAC	O	VMMC_3P3V	I^2S transmit data
X1A54	X_GPIO0	I/O	VMMC_3P3V	General purpose input/output 0 (GPIO1_24 of AM335x)
X1A55	X_GPIO1	I/O	VMMC_3P3V	General purpose input/output 1 (P0 from GPIO Exp. U2)
X1A56	X_GPIO2	I/O	VMMC_3P3V	General purpose input/output 2 (P1 from GPIO Exp. U2)
X1A57	reference-voltage	REF_O	VMMC_3P3V	GPIO reference voltage
X1A58	GND	-	-	Ground 0 V
X1A59	X_GPIO3	I/O	VMMC_3P3V	General purpose input/output 3 (P2 from GPIO Exp. U2)
X1A60	X_GPIO4	I/O	VMMC_3P3V	General purpose input/output 4 (P3 from GPIO Exp. U2)

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage domain	Description
X1A61	X_GPIO5	I/O	VMMC_3P3V	General purpose input/output 5 (GPIO1_23 of AM335x)
X1A62	X_GPIO6	I/O	VMMC_3P3V	General purpose input/output 6 (GPIO3_7 of AM335x)
X1A63	X_GPIO7	I/O	VMMC_3P3V	General purpose input/output 7 (P4 from GPIO Exp. U2)
X1A64	GND	-	-	Ground 0 V
X1A65	X_GPIO8	I/O	VMMC_3P3V	General purpose input/output 8 (P5 from GPIO Exp. U2)
X1A66	X_GPIO9	I/O	VMMC_3P3V	General purpose input/output 9 (P6 from GPIO Exp. U2)
X1A67	X_GPIO10	I/O	VMMC_3P3V	General purpose input/output 10 (P7 from GPIO Exp. U2)
X1A68	X_I2C0_SDA	OC-BI	VMMC_3P3V	I2C0 data
X1A69	X_I2C0_SCL	OC-BI	VMMC_3P3V	I2C0 clock
X1A70	GND	-	-	Ground 0 V
X1A71	reference-voltage	REF_O	VMMC_3P3V	I2C0 reference voltage
X1A72	X_nPM_RESET_IN	IPU	VDD_PM	Reset input
X1A73	X_nPM_RESET_OUT	OC	-	Reset output
X1A74	X_PM_SDA	OC-BI	VMMC_3P3V	Power management bus data (EMIC)
X1A75	X_PM_SCL	OC-BI	VMMC_3P3V	Power management bus clock (EMIC)
X1A76	GND	-	-	Ground 0 V
X1A77	X_nPM_ON/WAKEUP/OFF	IPU	VMMC_3P3V	Power on/wakeup/power off input
X1A78	X_PM_PWR_GOOD	OC	-	Power good output
X1A79	X_PM_PWM	OC	-	Fan PWM output (EMIC)
X1A80	X_PM_TACHO	5V_PD	-	Fan tacho input (EMIC)

Table 3: Pinout of the phyFLEX-fix Connector X1, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B1	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B2	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B3	VDD_5V_IN_R	PWR_I	5V	5 V Primary Voltage Supply Input
X1B4	GND	-	-	Ground 0 V
X1B5	reference-voltage	REF_O	VMMC_3P3V	JTAG reference voltage
X1B6	RSVD	-	-	reserved for future use
X1B7	GND	-	-	Ground 0 V
X1B8	reference-voltage	REF_O	VAUX2_3P3V	SD0 reference voltage
X1B9	X_SD0_WP	I	VDD_SD0	SD0 write protection
X1B10	X_nSD0_CD	I	VDD_SD0	SD0 card detection (active low)
X1B11	X_SD0_D3	I/O	VDD_SD0	SD0 data 3
X1B12	X_SD0_CMD	O	VDD_SD0	SD0 command
X1B13	GND	-	-	Ground 0 V
X1B14	X_SD0_CLK	O	VDD_SD0	SD0 clock
X1B15	X_SD0_D0	I/O	VDD_SD0	SD0 data 0
X1B16	X_SD0_D1	I/O	VDD_SD0	SD0 data 1
X1B17	X_SD0_D2	I/O	VDD_SD0	SD0 data 2
X1B18	-	-	-	nc
X1B19	GND	-	-	Ground 0 V
X1B20	-	-	-	nc
X1B21	-	-	-	nc
X1B22	-	-	-	nc
X1B23	RSVD	-	-	reserved for future use
X1B24	X_ETH0_ANALOG_VOLTAGE	REF_I	-	ETH0 reference voltage for 10/100 Mbit[1]
X1B25	GND	-	-	Ground 0 V
X1B26	X_ETH0_A+/TX0+	ETH_O	VMMC_3P3V	ETH0 data A+ /transmit+
X1B27	X_ETH0_A-/TX0-	ETH_O	VMMC_3P3V	ETH0 data A-/transmit-
X1B28	X_ETH0_LED0	OC	VMMC_3P3V	ETH0 link LED output
X1B29	X_ETH0_B+/RX0+	ETH_I	VMMC_3P3V	ETH0 data B+/receive+
X1B30	X_ETH0_B-/RX0-	ETH_I	VMMC_3P3V	ETH0 data B-/receive-
X1B31	GND	-	-	Ground 0 V

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B

[1]: for phyFLEX-AM335x this pin is only connected to a 100 nF capacitor tied to ground

Pin #	Signal	ST	Voltage Domain	Description
X1B32	X_ETH0_C+	ETH_I/O	VMMC_3P3V	ETH0 data C+ (only GbE)
X1B33	X_ETH0_C-	ETH_I/O	VMMC_3P3V	ETH0 data C- (only GbE)
X1B34	X_ETH0_LED1	OC	VMMC_3P3V	ETH0 traffic LED output
X1B35	X_ETH0_D+	ETH_I/O	VMMC_3P3V	ETH0 data D+ (only GbE)
X1B36	X_ETH0_D-	ETH_I/O	VMMC_3P3V	ETH0 data D- (only GbE)
X1B37	GND	-	-	Ground 0 V
X1B38	X_USB0_D-	USB_I/O	AM335 internal	USB0 data-
X1B39	X_USB0_D+	USB_I/O	AM335 internal	USB0 data+
X1B40	X_USB0_ID	I	VMMC_3P3V	USB0 ID Pin
X1B41	-	-	-	not connected
X1B42	-	-	-	not connected
X1B43	GND	-	-	Ground 0 V
X1B44	X_USB1_D-	USB_/IO	AM335 internal	USB1 data-
X1B45	X_USB1_D+	USB_I/O	AM335 internal	USB1data+
X1B46	RSVD	-	-	reserved for future use
X1B47	-	-	-	not connected
X1B48	-	-	-	not connected
X1B49	GND		-	Ground 0 V
X1B50	X_LVDS0_L0+	LVDS_O	AM335 internal	LVDS0 data0+
X1B51	X_LVDS0_L0-	LVDS_O	AM335 internal	LVDS0 data0-
X1B52	X_nLVDS0_DISP_EN	I/O	VMMC_3P3V	LVDS0 display enable (low active)
X1B53	X_LVDS0_L1+	LVDS_O	VDD_3V3	LVDS0 data1+
X1B54	X_LVDS0_L1-	LVDS_O	VDD_3V3	LVDS0 data1-
X1B55	GND	-	-	Ground 0 V
X1B56	X_LVDS0_L2+	LVDS_O	VDD_3V3	LVDS0 data2+
X1B57	X_LVDS0_L2-	LVDS_O	VDD_3V3	LVDS0 data2-
X1B58	X_LVDS0_DISP_BL_PWM	O	VMMC_3P3V	LVDS0 backlight PWM output
X1B59	X_LVDS0_L3+	LVDS_O	VDD_3V3	LVDS0 data3+

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X1B60	X_LVDS0_L3-	LVDS_0	VDD_3V3	LVDS0 data3-
X1B61	GND	-	-	Ground 0 V
X1B62	X_LVDS0_CLK+	LVDS_0	VDD_3V3	LVDS0 clock+
X1B63	X_LVDS0_CLK-	LVDS_0	VDD_3V3	LVDS0 clock-
X1B64	reference-voltage	REF_0	VMMC_3P3V	LVDS0 reference voltage
X1B65	-	-	-	not connected
X1B66	-	-	-	not connected
X1B67	GND	-	-	Ground 0 V
X1B68	-	-	-	not connected
X1B69	-	-	-	not connected
X1B70	-	-	-	not connected
X1B71	-	-	-	not connected
X1B72	-	-	-	not connected
X1B73	GND	-	-	Ground 0 V
X1B74	-	-	-	not connected
X1B75	-	-	-	not connected
X1B76	X_BOOT0	IPU	VDD_PM	Boot configuration 0
X1B77	X_BOOT1	IPU	VDD_PM	Boot configuration 1
X1B78	X_BOOT2	IPU	VDD_PM	Boot configuration 2
X1B79	GND	-	-	Ground 0 V
X1B80	RSVD	-	-	reserved for future use

Table 4: Pinout of the phyFLEX-fix Connector X1, Row B (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2A1	-	-	-	not connected
X2A2	-	-	-	not connected
X2A3	-	-	-	not connected
X2A4	X_CAN0_TXD	O	VMMC_3P3V	CAN0 transmit
X2A5	X_CAN0_RXD	I	VMMC_3P3V	CAN0 receive
X2A6	GND	-	-	Ground 0 V
X2A7	reference-voltage	REF_O	VMMC_3P3V	CAN reference voltage
X2A8	-	-	-	not connected
X2A9	-	-	-	not connected
X2A10	-	-	-	not connected
X2A11	-	-	-	not connected
X2A12	GND	-	-	Ground 0 V
X2A13	-	-	-	not connected
X2A14	-	-	-	not connected
X2A15	-	-	-	not connected
X2A16	-	-	-	not connected
X2A17	-	-	-	not connected
X2A18	GND	-	-	Ground 0 V
X2A19	-	-	-	not connected
X2A20	-	-	-	not connected
X2A21	-	-	-	not connected
X2A22	-	-	-	not connected
X2A23	-	-	-	not connected
X2A24	GND	-	-	Ground 0 V
X2A25	-	-	-	not connected
X2A26	-	-	-	not connected
X2A27	-	-	-	not connected
X2A28	-	-	-	not connected
X2A29	-	-	-	not connected
X2A30	GND	-	-	Ground 0 V
X2A31	-	-	-	not connected
X2A32	-	-	-	not connected
X2A33	-	-	-	not connected
X2A34	-	-	-	not connected

Table 5: Pinout of the phyFLEX-optional Connector X2, Row A

Pin #	Signal	ST	Voltage Domain	Description
X2A35	-	-	-	not connected
X2A36	GND	-	-	Ground 0 V
X2A37	-	-	-	not connected
X2A38	-	-	-	not connected
X2A39	-	-	-	not connected
X2A40	-	-	-	not connected
X2A41	-	-	-	not connected
X2A42	GND	-	-	Ground 0 V
X2A43	-	-	-	not connected
X2A44	-	-	-	not connected
X2A45	-	-	-	not connected
X2A46	-	-	-	not connected
X2A47	-	-	-	not connected
X2A48	GND	-	-	Ground 0 V
X2A49	-	-	-	not connected
X2A50	-	-	-	not connected

Table 5: Pinout of the phyFLEX-optional Connector X2, Row A (continued)

Pin #	Signal	ST	Voltage Domain	Description
X2B1	-	-	-	not connected
X2B2	-	-	-	not connected
X2B3	GND	-	-	Ground 0 V
X2B4	-	-	-	not connected
X2B5	-	-	-	not connected
X2B6	-	-	-	not connected
X2B7	-	-	-	not connected
X2B8	-	-	-	not connected
X2B9	GND	-	-	Ground 0 V
X2B10	-	-	-	not connected
X2B11	-	-	-	not connected
X2B12	-	-	-	not connected
X2B13	-	-	-	not connected
X2B14	X_ETH1_ANALOG_VOLTAGE	REF_I	-	ETH1 reference voltage 10/100 Mbit[1]
X2B15	GND	-	-	Ground 0 V
X2B16	X_ETH1_TX0+	ETH_O	VMMC_3P3V	ETH1 data A+ /transmit+
X2B17	X_ETH1_TX0-	ETH_O	VMMC_3P3V	ETH1 data A- /transmit-
X2B18	X_ETH1_LED0	OC	VMMC_3P3V	ETH1 link LED output
X2B19	X_ETH1_RX0+	ETH_I	VMMC_3P3V	ETH1 data B+/receive+
X2B20	X_ETH1_RX0-	ETH_I	VMMC_3P3V	ETH1 data B-/receive-
X2B21	GND	-	-	Ground 0 V
X2B22	-	-	-	not connected
X2B23	-	-	-	not connected
X2B24	X_ETH1_LED1	OC	VMMC_3P3V	ETH1 traffic LED output
X2B25	-	-	-	not connected
X2B26	-	-	-	not connected
X2B27	GND	-	-	Ground 0 V
X2B28	-	-	-	not connected
X2B29	-	-	-	not connected
X2B30	RSVD	-	-	reserved for future use
X2B31	-	-	-	not connected
X2B32	-	-	-	not connected

Table 6: Pinout of the phyFLEX-optional Connector X2, Row B

[1]: for phyFLEX-AM335x this pin is only connected to a 100 nF capacitor tied to ground

Pin #	Signal	ST	Voltage Domain	Description
X2B33	GND	-	-	Ground 0 V
X2B34	-	-	-	not connected
X2B35	-	-	-	not connected
X2B36	RSVD	-	-	reserved for future use
X2B37	-	-	-	not connected
X2B38	-	-	-	not connected
X2B39	GND	-	-	Ground 0 V
X2B40	-	-	-	not connected
X2B41	-	-	-	not connected
X2B42	RSVD	-	-	reserved for future use
X2B43	-	-	-	not connected
X2B44	-	-	-	not connected
X2B45	GND	-	-	Ground 0 V
X2B46	-	-	-	not connected
X2B47	-	-	-	not connected
X2B48	-	-	-	not connected
X2B49	-	-	-	not connected
X2B50	-	-	-	not connected

Table 6: Pinout of the phyFLEX-optional Connector X2, Row B (continued)

3 Jumpers

For configuration purposes, the phyFLEX-AM335x has several solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the solder jumper pads, while *Figure 6* and *Figure 7* indicate the location of the solder jumpers on the board. *Table 7* below provides a functional summary of the solder jumpers which can be changed to adapt the phyFLEX-AM335x to your needs. It shows their default positions, and possible alternative positions and functions. A detailed description of each solder jumper can be found in the applicable chapter listed in the table.

Note:
Jumpers not listed should not be changed as they are installed with regard to the configuration of the phyFLEX-AM335x.

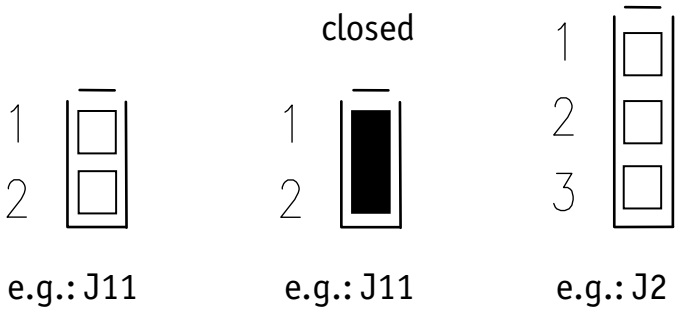


Figure 5: Typical Jumper Pad Numbering Scheme

If manual jumper modification is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

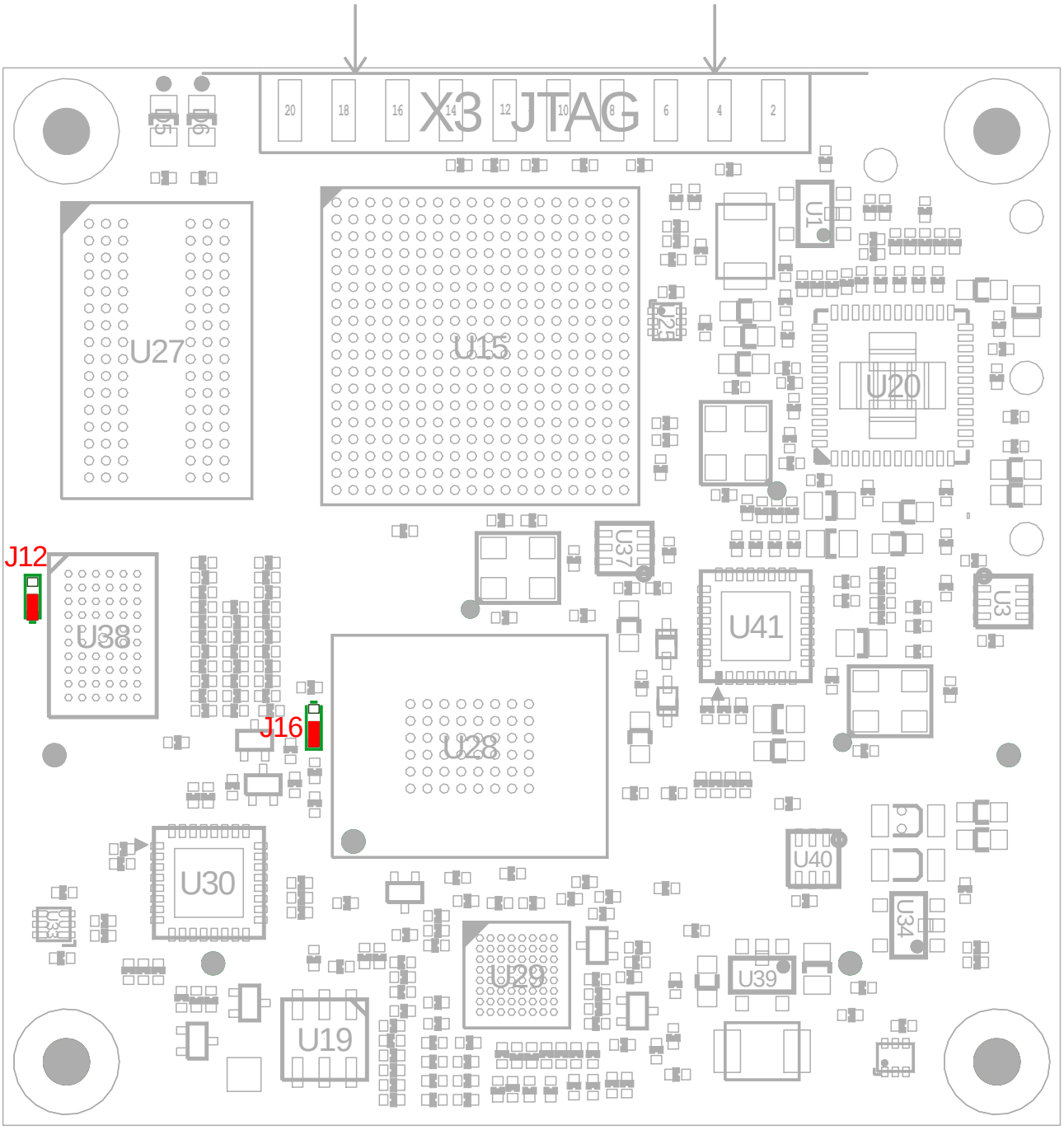


Figure 6: Jumper Locations (top view)

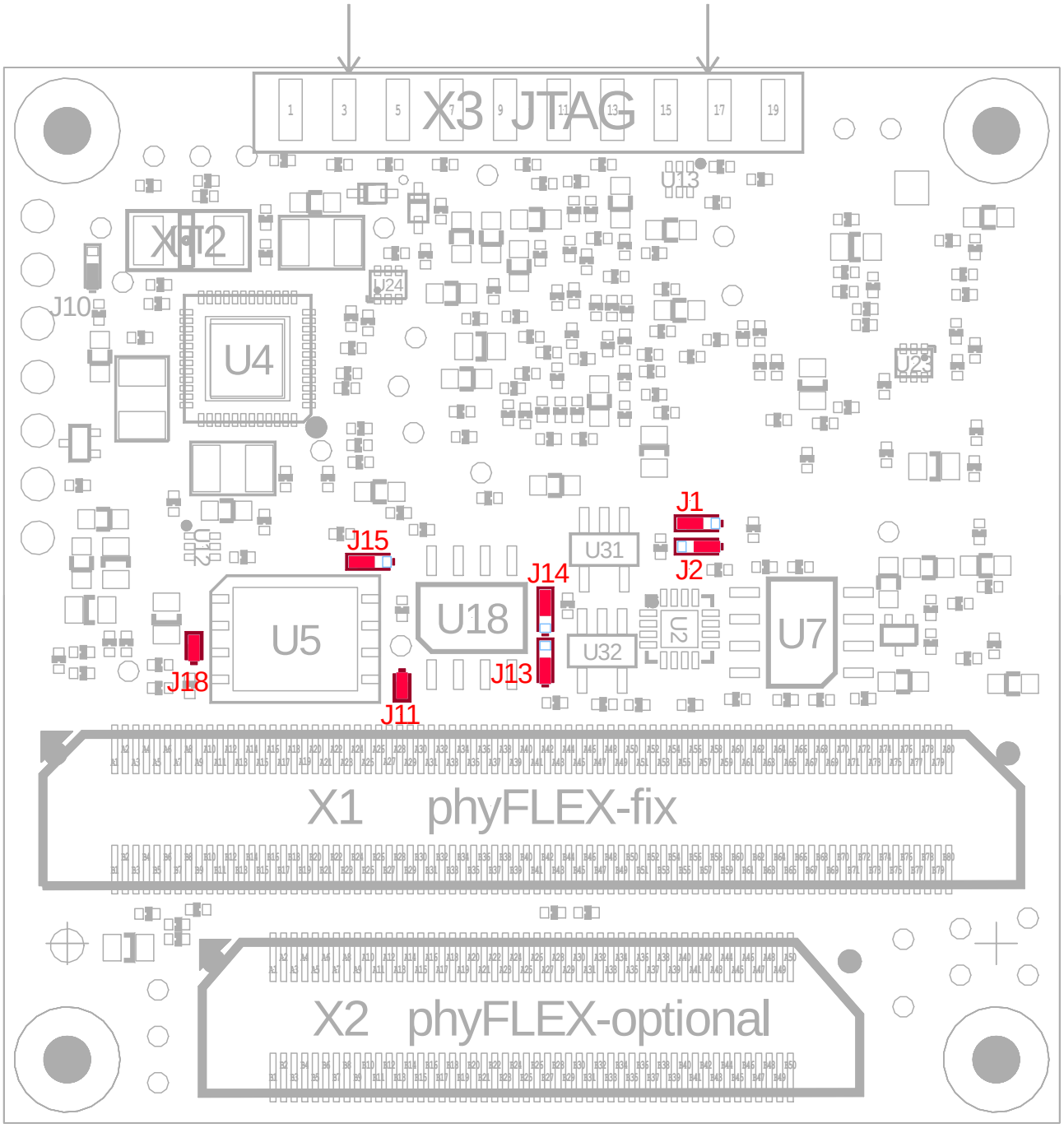


Figure 7: Jumper Locations (bottom view)

Please pay special attention to the "TYPE" column to ensure you are using the correct type of jumper (0 Ohms, 10k Ohms, etc...). The jumpers are either 0805 package or 0402 package with a 1/8 W or better power rating.

The jumpers (J = solder jumper) have the following functions:

Jumper	Description	Type	Chapter
J1,J2	J1 and J2 define the I²C address of the GPIO Expander providing GPIOs 1 to 4 and 7 to 10	0 Ohm (0402)	*9*
J1: 2+3 J2: 1+2	**A0 = SDA, A1 = SCL → I²C address 0x19**		
other settings	please refer to *Table 27* to find alternative addresses resulting from other combinations of jumpers J1 and J2		
J11	J11 connects pin 7 of the serial memory at U18 to GND. On many memory devices pin 7 enables/disables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyFLEX-AM335x will have this write protection function. *Please refer to the corresponding memory data sheet for more detailed information.*	0 Ohm (0402)	*6.3.2*
closed	**EEPROM is not write protected**		
open	EEPROM is write protected		
J12	J12 selects rising, or falling edge strobe for the LVDS Transmitter at U38 used for the display connectivity of the phyFLEX-AM335x.	0 Ohm (0402)	*11.1*
1+2	**falling edge strobe used for the LVDS display signals**		
2+3	rising edge strobe used for the LVDS display signals		
J13,J14	J13 and J14 define the slave addresses (A1 and A2) of the serial memory U18 on the I²C2 bus. In the high-nibble of the address, I²C memory devices have the slave ID 0x5. The low-nibble is build from A2, A1, A0 and the R/W bit.	0 Ohm (0402)	*6.3.1*
J13: 1+2 J14: 2+3	**A0 = 0, A1 = 1, A2= 0, => 0x2 / 0x3 (W/R) are selected as the low-nibble of the EEPROM's address → I²C address 0x52**		
other settings	please refer to *Table 11* to find alternative addresses resulting from other combinations of jumpers J13 and J14		

Table 7: Jumper Settings[1]

[1]: Defaults settings are in **bold blue** text

Jumper	Description	Type	Chapter
J15	J15 configures the enable or disable state of the SPI Flash device U5	0 Ohm (0402)	6.4.2
1+2	SPI Flash (U5) disabled		
2+3	**SPI Flash (U5) enabled**		
J16	J16 configures the write protection pin of the NAND Flash device U28	0 Ohm (0402)	6.2.1
1+2	write protection of the NAND Flash device U28 permanently enabled		
2+3	**write protection of the NAND Flash device U28 is only enabled during RESET**		
J18	J18 configures the write protection pin of the SPI Flash device U5	0 Ohm (0402)	6.4.1
closed	**Write protection disabled**		
open	Write protection enabled		

Table 7: Jumper Settings[1] (continued)

[1]: Defaults settings are in **bold blue** text

4 Power

The phyFLEX-AM335x operates off of a single power supply voltage.

The following sections of this chapter discuss the primary power pins on the phyFLEX-Connector X1 in detail.

4.1 Primary System Power (VDD_5V_IN_R)

The phyFLEX-AM335x operates off of a primary voltage supply with a nominal value of +5 V. On-board switching regulators generate the 3.3 V, 1.8 V, 1.5 V, and 1.1 V voltage supplies required by the AM335x MCU and on-board components from the primary 5 V supplied to the SOM.

For proper operation the phyFLEX-AM335x must be supplied with a voltage source of 5 V ±5 % with 2 A load at the VCC pins on the phyFLEX-Connector X1.

VDD_5V_IN_R: X1 A1, A2, A3, B1, B2, B3

Connect all +5 V VCC input pins to your power supply and at least the matching number of GND pins.

Corresponding GND: X1 A4, A10, A16, B4, B7, B13

Please refer to *section 2* for information on additional GND Pins located at the phyFLEX-Connector X1.

Caution!
As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry. For maximum EMI performance all GND pins should be connected to a solid ground plane.

4.2 Power Management IC (PMIC) (U4)

The phyFLEX-AM335x provides an on-board Power Management IC (PMIC) at position U4 to generate different voltages required by the processor and the on-board components. *Figure 8* presents a graphical depiction of the powering scheme.

The PMIC supports many functions like on-chip RTC and different power management functionalities like dynamic voltage control, different low power modes and regulator supervision. It is connected to the AM335x via the on board I^2C bus. The I^2C address of the PMIC is 0x2D (7 MSB). The smart reflex address is 0x12 (7 MSB).

Please refer to the Texas Instruments TPS65910A3 datasheet for further information.

4.2.1 Power Domains

External voltages:

- VDD_5V_IN_R 5 V main supply voltage
- USB0_VBUS USB0 Bus voltage, must be supplied with 5 V if USB0 is used
- USB1_VBUS USB1 Bus voltage, must be supplied with 5 V if USB1 is used

Internal voltages:
VDD_5V_IN[1] : only used to generate other voltages

Internally generated voltages:

VDD_CORE_1V1 (0.93 V-1.1V), VDD1_1P1V (0.93 V-1.1V), VDDR_1P5V (1.425 V-1.575 V), VDAC_1P8V (1.8 V), VPLL_1P8V(1.8 V), VDIG2_1P8V (1.8 V), VDIG1_1P8V(1.8 V), VAUX1_1P8V(1.8 V), VAUX33_3P3V (3.3 V), VAUX2_3P3V (3.3 V), VMMC_3P3V (3.3 V), VDD_PM(3.3 V), VDD_3V3(3.3 V)

- VDD_CORE_1V1 (0.93 V-1.1V) AM335x core
- VDD1_1P1V (0.93 V-1.1V) AM335x mpu
- VDDR_1P5V (1.425 V-1.575 V) AM335 EMIF(VDDS_DDR1...7), DDR3
- VDAC_1P8V (1.8 V) AM335x VDDs (VDDS1...7)
- VPLL_1P8V (1.8 V) AM335 VDDA_ADC
- VDIG2_1P8V (1.8 V) AM335 (VDDS_OSC, VDDS_PLL_CORE_LCD VDDS_PLL_DDR, VDDS_PLL_MPU)
- VDIG1_1P8V (1.8 V) AM335 VDDS_RTC
- VAUX2_3P3V (3.3 V) AM335 (VDDSHV2, VDDSHV4), SD0_VREF
- VMMC_3P3V (3.3 V) AM335 (VDDSHV1, VDDSHV3, VDDSHV5...6), VREF, IO-Voltage
- VDD_PM (3.3 V) DVCC MSP430G2253I (U30)
- VDD_3V3 (3.3 V) Peripherie Supply Voltage

[1]: derived from VDD_5V_IN_R via current sense amplifier at U16

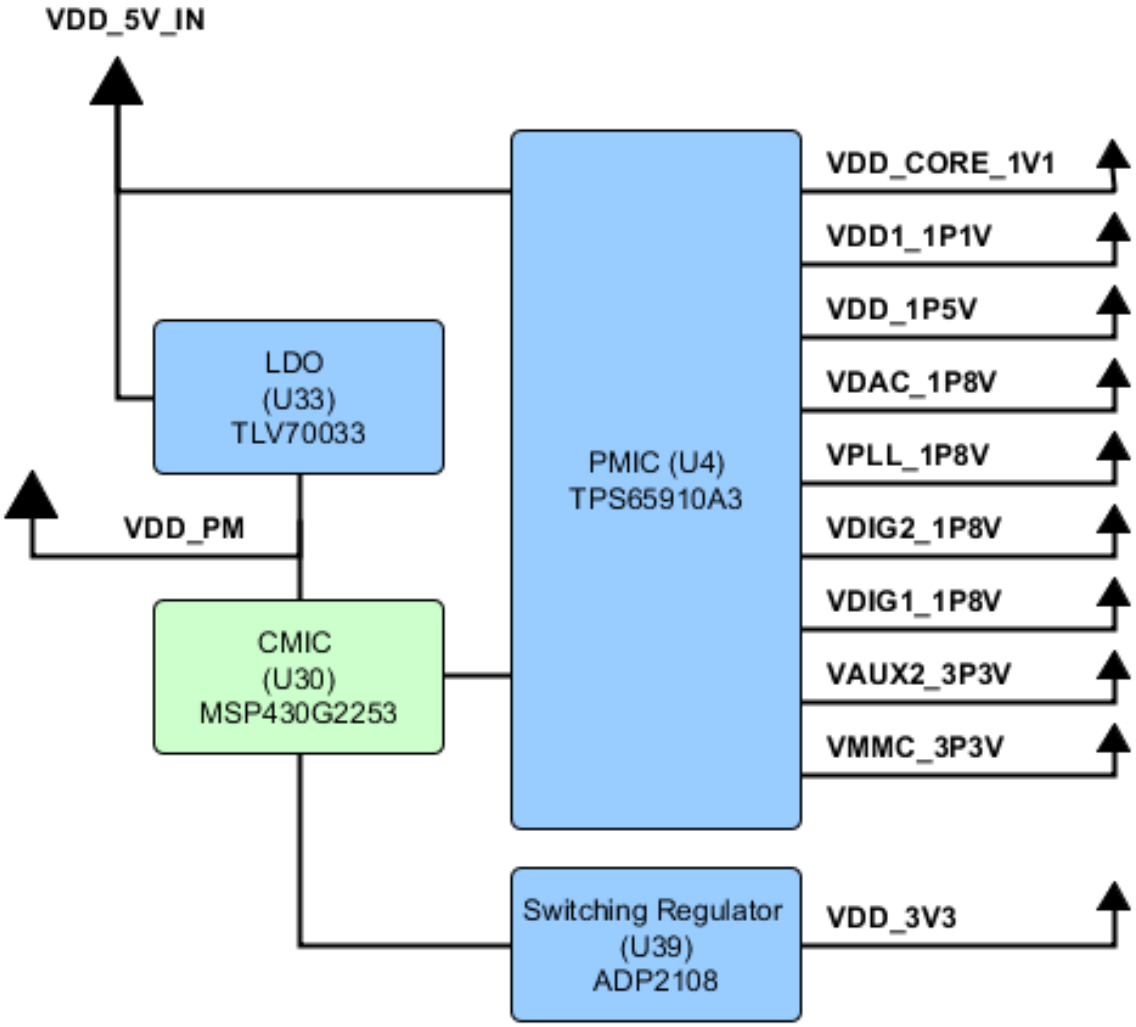


Figure 8: Powering scheme of phyFLEX- AM335x

4.3 Supply Voltage for external Logic

The voltage level of the phyFLEX's logic circuitry is VMMC_3P3V with 3.3 V (VAUX2_3P3V for SD0) which is generated on-board. In order to allow connecting external devices to the phyFLEX-AM335x without the need of another voltage source in addition to the primary supply this voltage is brought out at the different reference voltage pins of the phyFLEX-Connector.

Use of level shifters supplied with VMMC_3P3V (VAUX2_3P3V) allows converting the signals according to the needs on the custom target hardware. Alternatively signals can be connected to an open drain circuitry with a pull-up resistor attached to VMMC_3P3V (VAUX2_3P3V). The maximum load for VMMC_3P3V (VAUX2_3P3V) is, according to the phyFLEX specification 50 mA. Consequently this voltage should only be used as reference and not for supplying purpose.

4.4 Control Management IC (CMIC) (U30)

The Control Management IC (MSP430G2253I) at U30 monitors the supply voltage and generates necessary control signals for the AM335x processor as a result of different input signals. The CMIC also manages the boot, reset, wakeup and poweroff signals.

4.4.1 Power On/Off Control

Input signal X_nPM_ON/WAKEUP/OFF (X1A77) allows to turn the phyFLEX-AM335x on and off. Pulling this signal low for less than 5 seconds will wake up the phyFLEX-AM335x module, or will turn on the system, if it is powered off. Pulling this signal low for more than 5 seconds will turn off the system without proper shut down of the operating system.

4.4.2 Reset Control

U30 generates a reset if a reset is applied at pin X1A72 of the phyFLEX-Connector, or if the PMIC at U4 senses a voltage drop on the primary supply voltage and generates a reset signal. In addition nRESET_PER can be pulled low also by the bidirectional WARMRSTn output of the AM335x. In all cases if the reset signal nRESET_PER is pulled low additional instances will be reset (e.g. on-chip RTC of AM335x).

4.4.3 Boot Control

The CMIC is able to overwrite the default configuration of the pull-up/pull-down circuitry of sys_boot[4:0] depending on the external boot mode inputs X_BOOT[2:0] (X1B78, X1B77 and X1B76). Please refer to *section 5* for further details.

Please refer to the phyFLEX specification for further information.

5 System Configuration and Booting

Although most features of the AM335x microcontroller are configured and/or programmed during the initialization routine, other features, which impact program execution, must be configured prior to initialization via pin termination.

The system start-up configuration includes:

(1) Clock configuration
(2) Boot device order configuration

During the reset cycle the operational system boot mode of the AM335x processor is determined by the configuration of fifteen SYSBOOT pins sys_boot[15:0] (LCD_D[15:0]). Pins sys_boot[4:0] are used to select interfaces or devices for the booting list, where sys_boot [5] switches the CLKOUT1 signal of AM335x processor on or off. Pins sys_boot[7:6] select the PHY mode for booting via EMAC whereby sys_boot[8] selects the data bus size for the boot device connected to GPMC bus. Sys_boot[9] configures the ECC handling and sys_boot[11:10] the mux handling of GPMC bus. Sys_boot[13:12] is a reserved bit field, which has to be set to '00' for normal operation whereby sys_boot[15:14] select the crystal frequency for main oscillator.
All sixteen pins are sampled and latched into the CONTROL_STATUS[23:16] and CONTROL_STATUS[10:0] SYS_BOOT register bit field during the execution of the ROM code.

The internal ROM code is the first code executed during the initialization process of the AM335x after POR. Besides the selection of the system boot mode (also based on the configuration of pins sys_boot[7:6]), the ROM code detects which boot devices the controller has to check by using the sys_boot[4:0] pin configuration. For peripheral boot devices, the ROM code polls the communication interface selected, initiates the download of the code into the internal RAM and triggers its execution from there. Peripheral booting is normally not applicable after a warm reset. For memory booting, the ROM code finds the bootstrap in permanent memories such as NAND-Flash or SD-Cards and executes it. Memory booting is normally applicable after a cold, or a warm reset. Please refer to the AM335x Reference Manual for more information.

A configuration circuitry (pull-up and pull-down resistors connected to sys_boot[15:0]) is located on the phyFLEX module, so no further settings are necessary. The boot configuration of pins sys_boot[4:0] on the standard phyFLEX-AM335x module with 128 MB NAND Flash is **0b10011**. Consequently, the system tries to boot from NAND-Flash first, and, in case of a failure, successively from NAND connected to I^2C, MMC0 and UART0. Pins sys_boot[7:5] are factory-set to **0b010**, meaning that the CLKOUT1 signal is disabled and and interface mode for EMAC boot is set to RMII. Pins sys_boot [15:8] are also preprogrammed that all other necessary boot settings match the hardware configuration. The default value of sys_boot pins [15:8] is **0b10000010.**

The on-board configuration circuitry of sys_boot[4:0] can be overwritten by pull-up, or pull-down resistors connected to the boot configuration pins X_BOOT[2:0] (X1B78, X1B77 and X1B76) of the phyFLEX-AM335x.

The boot mode inputs X_BOOT[2:0] (X1B78, X1B77 and X1B76) are connected to the Control Management IC U30 and allow to change the booting device list. If left open X_BOOT[2:0] are high (memory boot).

The following tables show the different boot device orders, which can be selected by configuring the three boot configuration pins, X_BOOT[2:0] of the phyFLEX-AM335x.

Boot Mode	X_BOOT2	X_BOOT1	X_BOOT0	Bootsource
0	1	1	1	On board memory (e.g. NAND, SSD, eMMC)
1 (optional)	1	1	0	SPI0
2 (optional)	1	0	1	alternative on board memory (e.g. SSD, eMMC)
3 (optional)	1	0	0	SD0 external
4 (optional)	0	1	1	Serial (UART or USB)
5 (optional)	0	1	0	SATA0
6 (optional)	0	0	1	USB0
7 (optional)	0	0	0	specific (e.g. PCIe, I2C, Ethernet……)

Table 8: Standard phyFLEX Boot Options

The phyFLEX-AM335x specific boot options are shown in the following table.

Boot Mode	X_BOOT2	X_BOOT1	X_BOOT0	Bootsource
0	1	1	1	**NAND**,(NANDI2C,MMC0,UART0)
1	1	1	0	**SPI0, CS0** (on board SPI Flash if populated, same as mode 2), (MMC0,EMAC1,UART0)
2	1	0	1	**SPI0, CS0** (on board SPI Flash if populated, same as mode 1), (MMC0,EMAC1,UART0)
3	1	0	0	**SD0**, (SPI0, UART0, USB0)
4	0	1	1	**UART0**, (SPI0, NAND, NANDI2C)
5	0	1	0	**No SATA available – Boot Mode 0 is aktiv**
6	0	0	1	**Serial USB OTG USB0**, (NAND, SPI0, MMC0)
7	0	0	0	**EMAC1 (ETH1)**, (XIP (MUX1), SPI0, NANDI2C)

Table 9: phyFLEX-AM335x specific Boot Options[1]

[1]: Defaults settings are in **bold blue** text

6 System Memory

The phyFLEX-AM335x provides three types of on-board memory:

- DDR3 RAM: 128 MB DDR3 SDRAM (up to 512 MB)[1]
- NAND Flash (VFBGA): 128 MB (up to 1 GB)[1]
- I²C-EEPROM: 4 kB[1]
- SPI Flash: 8 MB[1]

The following sections of this chapter detail each memory type used on the phyFLEX-AM335x.

6.1 DDR3-SDRAM (U27)

The RAM memory of the phyFLEX-AM335x is comprised of a 16-bit wide DDR3-SDRAM chip at U27. The chip is connected to the special DDR3 interface called extended memory interface (EMIF) of the AM335x processor.

The DDR3-SDRAM memory is accessed via the EMIF SDRAM port starting at 0x8000 0000.

Typically the DDR3-SDRAM initialization is performed by a boot loader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or boot loader, SDRAM must be initialized by accessing the appropriate SDRAM configuration registers on the AM335x controller. Refer to the AM335x Reference Manual for accessing and configuring these registers.

6.2 NAND Flash Memory (U28)

Use of Flash as non-volatile memory on the phyFLEX-AM335x provides an easily reprogrammable means of code storage. The following Flash devices can be used on the phyFLEX-AM335x:

These Flash devices are programmable with 1.8 V. No dedicated programming voltage is required.

As of the printing of this manual these NAND Flash devices generally have a life expectancy of at least 100,000 erase/program cycles and a data retention rate of 10 years.

The NAND Flash memories are connected to the general-purpose memory controller (GPMC). /CS0 (GPMC_CS0n) of the GPMC interface selects the NAND Flash at U28.

[1]: Please contact PHYTEC for more information about additional module configurations.

6.2.1 NAND Flash Write Protection Control (J16)

Jumper J16 controls the write protection feature of the NAND Flash at U28. Setting this jumper to position 2 + 3 protects the flash against write access during a power on reset cycle. Setting this jumper to 1 + 2 protects the NAND Flash continuously against write cycles.

The following configurations are possible:

NAND Flash Write Protection State	J16
Write protection enabled during power on reset	**2 + 3**
continuously enabled write protection	1 + 2

Table 10: NAND Flash Write Protection via J16[1]

6.3 I²C EEPROM (U18)

The phyFLEX-AM335x is populated with a Catalyst 24C32WI[2] non-volatile 4 KB EEPROM with an I²C interface at U18. This memory can be used to store configuration data or other general purpose data. This device is accessed through I²C port 0 on the AM335x.

Write protection to the device is accomplished via jumper J11. Refer to *section 6.3.2* for further details.

6.3.1 Setting the EEPROM Address Bits (J13, J14)

The 32 KB I²C EEPROM populating U18 on the phyFLEX-AM335 module has the capability of configuring the address bits A1 and A2. The four upper address bits of the device are fixed at '1010' (see CAT24C32WI data sheet). A0 is fixed connected to GND. The remaining two lower address bits of the seven bit I²C device address are configurable using jumpers J13 and J14. J14 sets address bit A1 and J13 address bit A2.

Table 11 below shows the resulting seven bit I²C device address for the four possible jumper configurations.

U18 I²C Device Address	J13	J14
1010 000 (0x50)	1 + 2	1 + 2
1010 010 (0x52)	**1 + 2**	**2 + 3**
1010 100 (0x54)	2 + 3	1 + 2
1010 110 (0x56)	2 + 3	2 + 3

Table 11: U18 EEPROM I²C Address via J13 and J14[1]

[1]: Defaults are in **bold blue** text
[2]: See the manufacturer's data sheet for interfacing and operation

6.3.2 EEPROM Write Protection Control (J11)

Jumper J11 controls write access to the EEPROM (U18) device. Closing this jumper allows write access to the device, while removing this jumper will cause the EEPROM to enter write protect mode, thereby disabling write access to the device.

The following configurations are possible:

EEPROM Write Protection State	J11
Write access allowed	**closed**
Write protected	open

Table 12: EEPROM write protection states via J11[1]

6.4 SPI Flash Memory (U5)

The optional SPI Flash Memory of the phyFLEX-AM335x at U5 can be used to store configuration data or any other general purpose data. Beside this it can also be used as boot device. The device is accessed through SPI0 CS0 on the AM335x. Please see the *AM335x Reference Manual* for detailed information on the registers.

As of the printing of this manual these SPI Flash devices generally have a life expectancy of at least 100,000+ erase/program cycles and a data retention rate of 20 years. This makes the SPI Flash a reliable and secure solution to store the first and second level bootloaders.

6.4.1 SPI Flash Memory Protection Control (J18)

Jumper J18 controls write access to the SPI Flash (U5) device. In default position (jumper closed) write access to the device is possible. Opening jumper J18 write protects the SPI Flash (U5).

SPI Flash Write Protection State	J18
Write access allowed	**closed**
Write protected	open

Table 13: SPI Flash write protection states via J18[1]

[1]: Defaults are in **bold blue** text

6.4.2 SPI Flash Memory enable/disable (J15)

Jumper J15 allows to disable the SPI Flash at U5. Pausing the serial communication with the SPI Flash might be usefull if e.g. the CS signal is needed to control other devices.

The following configurations are possible:

SPI Flash Memory enable/disableNAND Flash Write Protection State	J15
SPI Flash enabled	**2 + 3**
SPI Flash disabled. Any serial communication with the device is paused, SO is at high impedance, and all input at SI and SCK are ignored.	1 + 2

Table 14: SPI Flash Memory enable/disable via J18[1]

[1]: Defaults are in **bold blue** text

7 SD / MM Card Interfaces

The phyFLEX bus features one fixed SD / MM Card interface and one optional SD / MM Card interface.. The phyFLEX-AM335x supports the fixed SD / MM Card interface only. The interface signals extend from the controllers first Multimedia Card High-speed/SD/SDIO (MMCHS) Host Controller to the phyFLEX-Connector. *Table 15* shows the location of the different interface signals on the phyFLEX-Connector. The MMC/SD/SDIO0 Host Controller is fully compatible with the SD Memory Card Specification 4.3 and SD I/O Specification 2.0. The phyFLEX-AM335x supports 4 of the host controller's 8 data channels with a maximum data rate of 192 Mbps (refer to the AM335x *Reference Manual* for more information). The MMCHS Host Controller is supplied by the VAUX2_3P3V voltage, which is created by the PMIC (U4) (3.3 V).

Because of compatibility reasons a card detect signal (X_nSD0_CD) is added to the SD / MMC Card Interface. This signal connects to GPIO1_17 of the AM335x processor.

Pin #	Signal	ST	Voltage Domain	Description
X1B8	reference-voltage	REF_O	VAUX2_3P3V	SD0 reference voltage
X1B9	X_SD0_WP	I	VDD_SD0	SD0 write protection (active high)
X1B10	X_SD0_nCD	I	VDD_SD0	SD0 card detection (active low); using GPIO1_17
X1B11	X_SD0_D3	I/O	VDD_SD0	SD0 data 3
X1B12	X_SD0_CMD	O	VDD_SD0	SD0 command
X1B14	X_SD0_CLK	O	VDD_SD0	SD0 clock
X1B15	X_SD0_D0	I/O	VDD_SD0	SD0 data 0
X1B16	X_SD0_D1	I/O	VDD_SD0	SD0 data 1
X1B17	X_SD0_D2	I/O	VDD_SD0	SD0 data 2

Table 15: Location of the SD / MM Card Interface Signals

Note:
If X_SD0_WP of the interface is not used (e.g. because a micro SD-Card slot is used) you should connect this signal to GND.

Please refer to the chapter "SD / MMC" in the phyFLEX Design-In Guide for more information about connecting an SD / MMC Card slot to the phyFLEX-AM335x.

8 Serial Interfaces

The phyFLEX-AM335x provides numerous serial interfaces some of which are equipped with a transceiver to allow direct connection to external devices:

1. Two high-speed UARTs (TTL, derived from UART0 and UART1 of the AM335x) with up to 3.6 Mbit/s and one with hardware flow control (RTS and CTS signals)
2. High-speed USB OTG interface (extended directly from the AM335x's USB-HS OTG PHY (USB-PHY))
3. High-speed USB HOST interface (extended directly from the AM335x USB HOST PHY (USB-PHY))
4. Two Auto-MDIX enabled Ethernet interfaces implemented using two Ethernet PHYs (one 10/100/1000 Mbit and one 10/100 Mbit) attached to the AM335x RGMII and RMII interface.
5. I^2C interface (derived from I^2C port 0 of the AM335x)
6. Two Serial Peripheral Interface (SPI) interface (extended from the first and second SPI module McSPI0 and McSPI1) of the AM335x)
7. I^2S audio interface (originating from the first module of the AM335x 's Multichannel Buffered Serial Port (McASP))
8. CAN 2.0B interface (extended directly from the AM335x DCAN1 module with up to 1 Mbit/s)

The following sections of this chapter detail each of these serial interfaces and any applicable configuration jumpers.

8.1 Universal Asynchronous Interface

The phyFLEX-AM335x provides two high-speed universal asynchronous interfaces with up to 3.6 Mbit/s and one with additional hardware flow control (RTS and CTS signals). The following table shows the location of the signals on the phyFLEX-Connector.

Pin #	Signal	ST	Voltage Domain	Description
X1A12	X_UART1_TXD	O	VMMC_3P3V	UART1 serial transmit signal
X1A13	X_UART1_RXD	I	VMMC_3P3V	UART1 serial data receive signal
X1A14	X_UART1_RTS	O	VMMC_3P3V	UART1 request to send
X1A15	X_UART1_CTS	I	VMMC_3P3V	UART1 clear to send
X1A17	reference-voltage	REF_O	VMMC_3P3V	UART1 reference voltage
X1A18	X_UART0_TXD	O	VMMC_3P3V	UART0 serial transmit signal
X1A19	reference-voltage	REF_O	VMMC_3P3V	UART0 reference voltage
X1A20	X_UART0_RXD	I	VMMC_3P3V	UART0 serial data receive signal

Table 16: Location of the UART Signals

The signals extend from UART1 respectively UART0 of the AM335x directly to the phyFLEX-Connector without conversion to RS-232 level. External RS-232 transceivers must be attached by the user if RS-232 levels are required.

8.2 USB OTG Interface

The phyFLEX-AM335x provides a high-speed USB OTG interface which uses the AM335x embedded HS USB OTG PHY (USB port USB0 of the AM335x). An external USB Standard-A (for USB host), USB Standard-B (for USB device), or USB mini-AB (for USB OTG) connector is all that is needed to interface the phyFLEX-AM335x USB OTG functionality. The applicable interface signals can be found on the phyFLEX-fix Connector X1 as shown in *Table 17*. The overcurrent pin is not supported by the AM335x muxing. If it is necessary to use this pins a softwaresolution to handle the overcurrent pin status is needed.

Pin #	Signal	ST	Voltage Domain	Description
X1A37	X_nUSB0_VBUSEN	O	VMMC_3P3V	USB0 VBUS enable (active low)
X1A38	X_USB0_VBUS	PWR_I	5V	USB0 VBUS input
X1A39	X_nUSB0_OC	I	VMMC_3P3V	USB0 overcurrent pin (GPIO1_30)
X1A41	reference-voltage	REF_O	VMMC_3P3V	USB0 reference voltage
X1A42	X_USB0_CHGDET	O	VMMC_3P3V	USB0 charger detection
X1B38	X_USB0_D-	USB_I/O	AM335x internal	USB0 data-
X1B39	X_USB0_D+	USB_I/O	AM335x internal	USB0 data+
X1B40	X_USB0_ID	I	VMMC_3P3V	USB0 ID Pin

Table 17: Location of the USB OTG Signals

8.3 USB Host Interface

The phyFLEX-AM335x provides a high-speed USB Host interface which uses the AM335x embedded HS USB Host PHY (USB port USB1 of the AM335x).

An external USB Standard-A (for USB host) connector is all that is needed to interface the phyFLEX-AM335x USB Host functionality. The applicable interface signals (D+/D-/ PWR/OC) can be found on the phyFLEX-fix Connector X1. The overcurrent pin is not supported by the AM335x muxing. If it is necessary to use this pins a softwaresolution to handle the overcurrent pin status is needed.

Pin #	Signal	ST	Voltage Domain	Description
X1A43	X_nUSB1_VBUSEN	O	VMMC_3P3V	USB1 VBUS enable (active low)
X1A44	X_USB1_VBUS	PWR_I	5V	USB1 VBUS input
X1A45	X_nUSB1_OC	I	VMMC_3P3V	USB1 overcurrent pin (GPIO1_31)
X1A47	reference-voltage	REF_O	VMMC_3P3V	USB1 reference voltage
X1B44	X_USB1_D-	USB_I/O	AM335x internal	USB1 data-
X1B45	X_USB1_D+	USB_I/O	AM335x internal	USB1 data+

Table 18: Location of the USB-Host Signals

8.4 Ethernet Interface

Connection of the phyFLEX-AM335x to the world wide web or a local area network (LAN) is possible by means of two Ethernet interfaces ETH0 and ETH1. The first Ethernet interface ETH0 is implemented by using the on-board GbE PHY at U20. The GbE PHY is connected to the RGMII1 interface of the AM335x and operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s or 1000 Mbit/s . The second Ethernet interface ETH1 is build with the FEC (Fast Ethernet Controller) at U41 . FEC PHY is connected to the RMII2 interface of the AM335 and supports data transmission at 10 Mbit/s or 100 Mbit/s.

8.4.1 Gigabit Ethernet PHY (ETH0)

With an Ethernet PHY mounted at U20 the phyFLEX-AM335x has been designed for use in 10Base-T, 100Base-T and 1000Base-T networks. The 10/100/1000Base-T interface with its LED signals extends to the phyFLEX-fix Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1B24	X_ETH0_ANALOG_ VOLTAGE	REF_O	VMMC_3P3V	ETH0 reference voltage for 10/100Mbit , for phyFLEX-AM335x this pin is only connected to a 100 nF capacitor tied to ground
X1B26	X_ETH0_A+/TX0+	ETH_O	VMMC_3P3V	ETH0 data A+ /transmit+
X1B27	X_ETH0_A-/TX0-	ETH_O	VMMC_3P3V	ETH0 data A-/transmit-
X1B28	X_ETH0_LED0	OC	VMMC_3P3V	ETH0 link LED output
X1B29	X_ETH0_B+/RX0+	ETH_I	VMMC_3P3V	ETH0 data B+/receive+
X1B30	X_ETH0_B-/RX0-	ETH_I	VMMC_3P3V	ETH0 data B-/receive-
X1B32	X_ETH0_C+	ETH_O	VMMC_3P3V	ETH0 data C+ (for GbE only)
X1B33	X_ETH0_C-	ETH_O	VMMC_3P3V	ETH0 data C- (for GbE only)
X1B34	X_ETH0_LED1	OC	VMMC_3P3V	ETH0 traffic LED output
X1B35	X_ETH0_D+	ETH_I/O	VMMC_3P3V	ETH0 data D+ (for GbE only)
X1B36	X_ETH0_D-	ETH_I/O	VMMC_3P3V	ETH0 data D- (for GbE only)

Table 19: Location of the Ethernet Signals (ETH0)

The on board GbE PHY supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an Auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet controller is connected to the RGMII1 interface of the AM335x. Please refer to the *AM335x Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100/1000Base-T network some external circuitry is required. The required termination resistors on the analog signals (ETH0_A±, ETH0_B±, ETH0_C±, ETH0_D±) are integrated in the chip, so there is no need to connect external termination resistors to these signals. Connection to an external Ethernet magnetics should be done using very short signal traces. The A+/A-, B+/B-, C+,C- and D+/D- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

If you are using the applicable carrier board for the phyFLEX-AM335x (part number PBA-B-01), the external circuitry mentioned above is already integrated on the board (refer to *section 15.3.5*).

Caution!
Please see the datasheet of the Ethernet PHY when designing the Ethernet transformer circuitry.

8.4.1.1 Reset of the Ethernet Controller (U20)

The Ethernet controller at U20 can be reset either by hardware, or software reset. The reset input of the Ethernet controller is permanently connected to the global reset signal nRESET_PER of the phyFLEX-AM335. A reset can be generated either by the CMIC U30 depending on the external signal X_nPM_RESET_IN at pin X1A72, or from the bidirectional WARMRSTn output of the AM335x processor.

8.4.2 Ethernet PHY (ETH1)

With an Ethernet PHY mounted at U41 the phyFLEX-AM335x has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED signals extends to the phyFLEX-optional Connector X2.

Pin #	Signal	ST	Voltage Domain	Description
X2B14	X_ETH1_ANALOG_ VOLTAGE	REF_O	VMMC_3P3V	ETH1 reference voltage for 10/100Mbit , for phyFLEX-AM335x this pin is only connected to a 100 nF capacitor tied to ground
X2B16	X_ETH1_TX0+	ETH_O	VMMC_3P3V	ETH1 data A+ /transmit+
X2B17	X_ETH1_TX0-	ETH_O	VMMC_3P3V	ETH1 data A-/transmit-
X2B18	X_ETH1_LED0	OC	VMMC_3P3V	ETH1 link LED output
X2B19	X_ETH1_RX0+	ETH_I	VMMC_3P3V	ETH1 data B+/receive+
X2B20	X_ETH1_RX0-	ETH_I	VMMC_3P3V	ETH1 data B-/receive-
X2B24	X_ETH1_LED1	OC	VMMC_3P3V	ETH1 traffic LED output

Table 20: Location of the Ethernet Signals (ETH1)

The on board FEC PHY supports HP Auto-MDIX technology, eliminating the need for the consideration of a direct connect LAN cable, or a cross-over patch cable. It detects the TX and RX pins of the connected device and automatically configures the PHY TX and RX pins accordingly. The Ethernet PHY also features an Auto-negotiation to automatically determine the best speed and duplex mode.

The Ethernet controller is connected to the RMII2 interface of the AM335x. Please refer to the *AM335x Reference Manual* for more information about this interface.

In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required termination resistors on the analog signals (ETH1_TX±, ETH1_RX±) are integrated in the chip, so there is no need to connect external termination resistors to these signals. Connection to an external Ethernet magnetics should be done using very short signal traces. The TX+/TX- and RX+/RX- signals should be routed as 100 Ohm differential pairs. The same applies for the signal lines after the transformer circuit. The carrier board layout should avoid any other signal lines crossing the Ethernet signals.

If you are using the applicable carrier board for the phyFLEX-AM335x (part number PBA-B-01), the external circuitry mentioned above is already integrated on the board (refer to *section 15.3.5*).

Caution!
Please see the datasheet of the Ethernet PHY when designing the Ethernet transformer circuitry.

8.4.2.1 Reset of the Ethernet Controller (U41)

The Ethernet controller at U41 can be reset either by hardware, or software reset. The reset input of the Ethernet controller is permanently connected to the global reset signal nRESET_PER of the phyFLEX-AM335. A reset can be generated either by the CMIC U30 depending on an external signal X_nPM_RESET_IN at pin X1A72, or from the bidirectional WARMRSTn output of the AM335x processor.

8.4.3 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. TI has acquired a pool of MAC addresses for their Sitara processor series. The MAC address of the phyCARD-AM335x is programmed via processor specific fuses from TI side, and can be read out by software. The Barebox, or the BSP reads out the unique MAC address and stores it in an appropriate variable as a 12-digit HEX value.

8.5 I²C Interface

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The AM335x contains three multimaster fast-mode I^2C modules. Module I2C0 connects to the I^2C components on the phyFLEX-AM335x and is available at the phyFLEX Connector, whereas the pins of the second and third module (I2C1 and I2C2) are assigned to other functions.

The control registers for I²C port 0 are mapped between addresses 0x44E0 B000 and 0x44E0 BFFF. Please see the *AM335x Reference Manual* for detailed information on the registers.

Module I2C0 is connected to the on-board EEPROM (U18) (*section 6.3),* GPIO Expander (U2) (*section 9)*, PMIC (U4) (*section 4.2)* and to the EMIC (U29) (*section 12*). The I^2C interface extends also to the phyFLEX Connector. An I^2C Buffer is used to ensure, that the I^2C interface at the phyFLEX-Connector is ready for a capacitive load of max. 150 pF in fast mode.

The following table lists the pins of the I^2C port on the phyFLEX-Connector.

Pin #	Signal	ST	Voltage Domain	Description
X1A68	X_I2C0_SDA	I/O	VMMC_3P3V	I2C0 data
X1A69	X_I2C0_SCL	I/O	VMMC_3P3V	I2C0 clock
X1A71	reference-voltage	REF_O	VMMC_3P3V	I2C0 reference voltage

Table 21: I^2C Interface Signal Location

To avoid any conflicts when connecting external I^2C devices to the phyFLEX AM335x the addresses of the on-board I^2C devices must be considered. On the SOM only I2C0 is used for the different devices. Some of the addresses can be configured by jumper. *Table 22* lists the addresses already in use. The table shows only the default address. Please refer to *section3* for alternative address settings.

Component	Address (7 MSB)	Jumper
EEPROM (U18)	0x52	J13, J14
GPIO Expander (U2)	0x19	J1, J2
PMIC (U4)	0x2D 0x12 (SmartReflex)	
EMIC (U29)	tbd.	

Table 22: I^2C addresses in Use

8.6 I^2S Audio Interface (SSI))

The Synchronous Serial Interface (SSI) of the phyFLEX-AM335x is a full-duplex, serial interface that allows to communicate with a variety of serial devices, such as standard codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I^2S) and Intel AC'97 standard. The AM335x provides two instances of the McASP module (McASP0 and McASP1). On the phyFLEX-AM335x McASP0 is brought out to the phyFLEX-Connector.

With reference to the phyFLEX specification, the main purpose of this interface is to connect to an external codec, such as I^2S. Four signals extend from the AM335x McASP0 module to the phyFLEX-Connector (I2S0_CLK, I2S0_FRM, I2S0_ADC, I2S0_DAC).

Pin #	Signal	ST	Voltage Domain	Description
X1A48	X_I2S0_CLK	I/O	VMMC_3P3V	I2S0 clock
X1A49	X_I2S0_FRM	I/O	VMMC_3P3V	I2S0 frame
X1A50	X_I2S0_ADC	I	VMMC_3P3V	I2S0 receive data
X1A51	reference-voltage	REF_O	VMMC_3P3V	I2S0 reference voltage
X1A53	X_I2S0_DAC	O	VMMC_3P3V	I2S0 transmit data

Table 23: I^2S Interface Signal Location

8.7 SPI Interface

The Serial Peripheral Interface (SPI) interface is a four-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyFLEX provides two SPI interfaces on the phyFLEX-fix connector X1. The SPI interfaces provide two chip select signals each. The multichannel serial port interfaces (McSPI) of the AM335x has two separate instantiations (SPI0 and SPI1). The interface signals of both modules (McSPI0 and McSPI1) are made available on the phyFLEX-fix Connector. The modules are master/slave configurable. The following table lists the SPI signals on the phyFLEX-Connector:

Pin #	Signal	ST	Voltage Domain	Description
X1A21	X_SPI0_MOSI	O	VMMC_3P3V	SPI0 master output/slave input
X1A23	X_SPI0_MISO	I	VMMC_3P3V	SPI0 master input/slave output
X1A24	X_SPI0_CSBOOT	O	VMMC_3P3V	SPI0 chip select BOOT (SPI0_CS0 of AM335x)
X1A25	X_SPI0_CS0	O	VMMC_3P3V	SPI0 chip select 0 (GPIO1_19 of AM335x)
X1A26	X_SPI0_CS1	O	VMMC_3P3V	SPI0 chip select 1 (SPI0_CS1 of AM335x)
X1A27	reference-voltage	REF_O	VMMC_3P3V	SPI0 reference voltage
X1A29	X_SPI0_CLK	O	VMMC_3P3V	SPI0 clock signal
X1A30	X_SPI1_CS0	O	VMMC_3P3V	SPI1 chip select 0
X1A31	X_SPI1_MOSI	O	VMMC_3P3V	SPI1 master output/slave input
X1A32	X_SPI1_MISO	I	VMMC_3P3V	SPI1 master input/slave output
X1A33	reference-voltage	REF_O	VMMC_3P3V	SPI1 reference voltage
X1A35	X_SPI1_CLK	O	VMMC_3P3V	SPI1 clock signal
X1A36	X_SPI1_CS1	O	VMMC_3P3V	SPI1 chip select 1 (GPIO1_18 of AM335x)

Table 24: SPI Interface Signal Location

Note:
If an SPI Flash is mounted at U5 it will be selected by X_SPI0_CSBOOT. In this case X_SPI0_CSBOOT can not be used on a custom carrier board.

8.8 CAN Interface

The CAN interface of the phyFLEX-AM335x is connected to the second DCAN module (DCAN1) of the AM335x which is a full implementation of the CAN protocol specification Version 2.0B. It supports standard and extended message frames and programmable bit rates of up to 1 Mb/s.

The signals of the CAN interface are brought out on the phyFLEX-optional connector X2. The following table shows the position of the signals.

Pin #	Signal	ST	Voltage Domain	Description
X2A4	X_CAN0_TXD	O	VMMC_3P3V	CAN0 transmit
X2A5	X_CAN0_RXD	I	VMMC_3P3V	CAN0 receive
X2A7	reference-voltage	REF	VMMC_3P3V	CAN reference voltage

Table 25: CAN Interface Signal Location

9 General Purpose I/Os

The phyFLEX bus provides 11 GPIO signals. GPIO0, GPIO5 and GPIO6 are ports of the AM335x, while GPIO1..4 and GPIO7..10 are realized using a GPIO Expander at U2. The GPIO Expander is accessible over I^2C on address 0x19. *Table 26* shows the location of the GPIO pins on the phyFLEX-Connector, as well as the corresponding ports of the AM335x or GPIO Expander.

Pin #	Signal	ST	Voltage Domain	Description
X1A54	X_GPIO0	I/O	VMMC_3P3V	General purpose input/output 0 (GPIO1_24 of AM335x)
X1A55	X_GPIO1	I/O	VMMC_3P3V	General purpose input/output 1 (P0 from GPIO Expander U2)
X1A56	X_GPIO2	I/O	VMMC_3P3V	General purpose input/output 2 (P1 from GPIO Expander U2)
X1A57	reference-voltage	REF_O	VMMC_3P3V	GPIO reference voltage
X1A59	X_GPIO3	I/O	VMMC_3P3V	General purpose input/output 3 (P2 from GPIO Expander U2)
X1A60	X_GPIO4	I/O	VMMC_3P3V	General purpose input/output 4 (P3 from GPIO Expander U2)
X1A61	X_GPIO5	I/O	VMMC_3P3V	General purpose input/output 5 (GPIO1_23 of AM335x)
X1A62	X_GPIO6	I/O	VMMC_3P3V	General purpose input/output 6 (GPIO3_7 of AM335x)
X1A63	X_GPIO7	I/O	VMMC_3P3V	General purpose input/output 7 (P4 from GPIO Expander U2)
X1A65	X_GPIO8	I/O	VMMC_3P3V	General purpose input/output 8 (P5 from GPIO Expander U2)
X1A66	X_GPIO9	I/O	VMMC_3P3V	General purpose input/output 9 (P6 from GPIO Expander U2)
X1A67	X_GPIO10	I/O	VMMC_3P3V	General purpose input/output 10 (P7 from GPIO Expander U2)

Table 26: Location of GPIO Pins

Note:
GPIOs from the GPIO Expander (U2) have only an internal pull-up for high level but they are not able to pull high level.

Beside these 11 dedicated GPIOs, most of the AM335x signals which are connected directly to the module connector can be configured to act as GPIOs, due to the multiplexing functionality of most controller pins.

9.1.1 Setting the GPIO Expander Address Bits (J1, J2)

Jumpers J1 and J2 allow to change the I^2C address of the GPIO Expander if necessary. The following table shows the possible I^2C addresses of the GPIO Expander.

U2 I²C Device Address	J2	J1
0011 000 (0x18)	1 + 2	1 + 2
0011 001 (0x19)	**1 + 2**	**2 + 3**
0011 010 (0x1A)	2 + 3	1 + 2
0011 011 (0x1B)	2 + 3	2 + 3

Table 27: U2 GPIO Expander I²C Address Configuration with J1 and J2[1]

[1]: Defaults are in **bold blue** text

10 Debug Interface (X1, X3)

The phyFLEX-AM335x is equipped with a JTAG interface for downloading program code into the external flash, internal controller RAM or for debugging programs currently executing. The JTAG interface extends to the phyFLEX-fix connector X1 and also to a 2.0 mm pitch pin header at X3 on the edge of the module PCB.

Table 28 shows the location of the JTAG pins on the phyFLEX-fix connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1A5	X_nJTAG_TRSTB	I	VMMC_3P3V	JTAG reset input
X1A6	X_JTAG_TDI	I	VMMC_3P3V	JTAG TDI
X1A7	X_JTAG_TMS	I	VMMC_3P3V	JTAG TMS
X1A8	X_JTAG_TDO	O	VMMC_3P3V	JTAG TDO
X1A9	X_JTAG_TCK	I	VMMC_3P3V	JTAG clock input
X1A10	GND	-	-	Ground 0 V
X1A11	X_JTAG_RTCLK	O	VMMC_3P3V	JTAG RTCLK (connected to X_JTAG_TCK via 0 Ohm resistor)
X1B5	reference-voltage	REF_O	VMMC_3P3V	JTAG reference voltage

Table 28: Debug Interface Signal Location at phyFLEX-Connector X1

Figure 9 and *Figure 10* show the position of the debug interface (JTAG connector X3) on the phyFLEX-AM335x module.

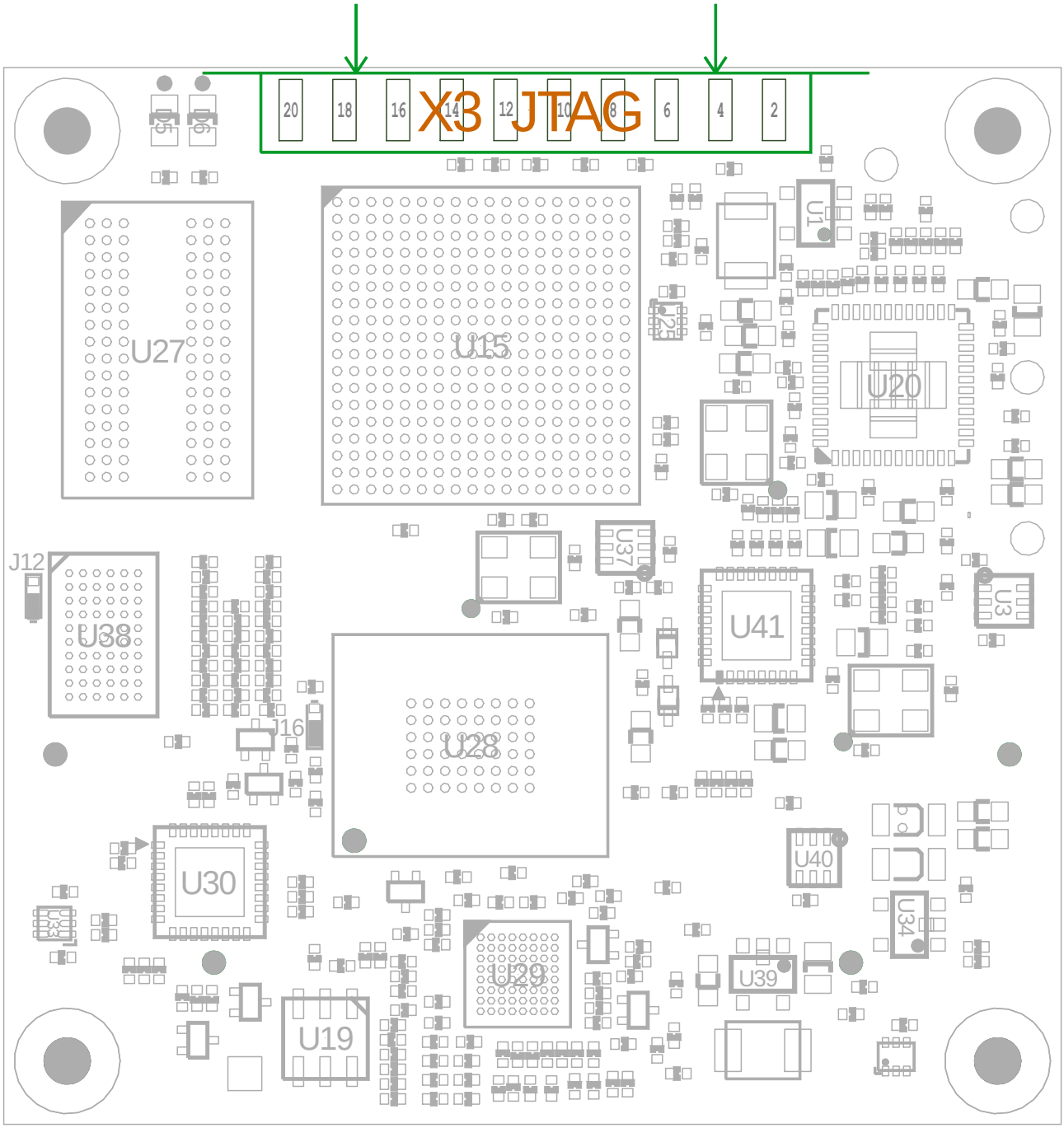


Figure 9: JTAG Interface X3 (top view)

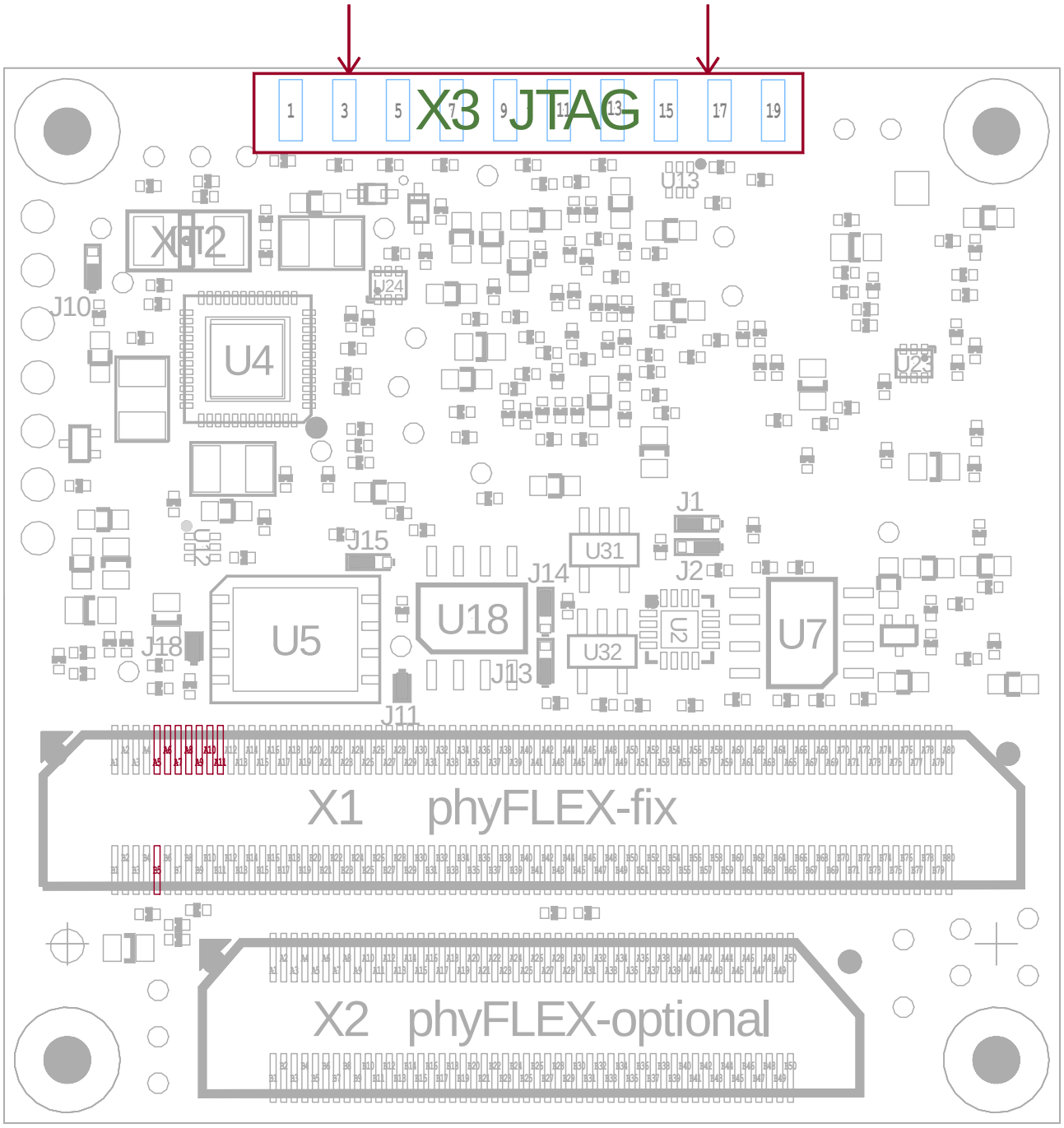


Figure 10: JTAG Interface X3 (bottom view)

Pin 1 of the JTAG connector X3 is on the connector side of the module. Pin 2 of the JTAG connector is on the controller side of the module.

Table 29 shows details on the JTAG signal pin assignment.

Note:
The JTAG connector X3 only populates phyFLEX-AM335x modules with a specific order option. We recommend integration of a standard (2 mm pitch) pin header connector in the user target circuitry to allow easy program updates via the JTAG interface.

Signal	Pin Row*		Signal
	A	B	
VSUPPLY (VMMC_3P3V)	2	1	TREF (VMMC_3P3V via 100 Ohm resistor)
GND	4	3	X_nJTAG_TRSTB
GND	6	5	X_JTAG_TDI
GND	8	7	X_JTAG_TMS
GND	10	9	X_JTAG_TCK
GND	12	11	X_JTAG_RTCK (connected to X_JTAG_TCK)
GND	14	13	X_JTAG_TDO
GND	16	15	X_nRESET_PER
GND	18	17	not connected
GND	20	19	not connected

Table 29: JTAG Connector X3 Signal Assignment

***Note:** Row A is on the controller side of the module and row B is on the connector side of the module

PHYTEC offers a JTAG-Emulator adapter (order code JA-002) for connecting the phyFLEX-AM335x to a standard emulator. The JTAG-Emulator adapter extends the signals of the module's JTAG connector to a standard ARM connector with 2 mm pin pitch. The JA-002 therefore functions as an adapter for connecting the module's non-ARM-compatible JTAG connector X3 to standard Emulator connectors.

11 LVDS Display Interface

The phyFLEX-AM335x uses a 4-Channel 24-Bit LVDS Transmitter (U38) to generate LVDS-Signals from the LCD Interface Display Driver (LIDD) controller of the AM335x. Thus an LVDS-Display can connect directly to the phyFLEX-AM335x. The location of the applicable interface signals (X_LVDS0_L0-3+, X_LVDS0_L0-3-, X_LVDS0_CLK+ and X_LVDS0_CLK-) and of the two control signals display enable and backlight PWM (X_nLVDS0_DISP_EN and X_LVDS0_DISP_BL_PWM) can be found in the table below.

Pin #	Signal	ST	Voltage Domain	Description
X1B50	X_LVDS0_L0+	LVDS_O	AM335 internal	LVDS0 data0+
X1B51	X_LVDS0_L0-	LVDS_O	AM335 internal	LVDS0 data0-
X1B52	X_nLVDS0_DISP_EN	O	VMMC_3P3V	LVDS0 display enable (low active)
X1B53	X_LVDS0_L1+	LVDS_O	AM335 internal	LVDS0 data1+
X1B54	X_LVDS0_L1-	LVDS_O	AM335 internal	LVDS0 data1-
X1B56	X_LVDS0_L2+	LVDS_O	AM335 internal	LVDS0 data2+
X1B57	X_LVDS0_L2-	LVDS_O	AM335 internal	LVDS0 data2-
X1B58	X_LVDS0_DISP_BL_PWM	O	VMMC_3P3V	LVDS0 backlight PWM output
X1B59	X_LVDS0_L3+	LVDS_O	AM335 internal	LVDS0 data3+
X1B60	X_LVDS0_L3-	LVDS_O	AM335 internal	LVDS0 data3-
X1B62	X_LVDS0_CLK+	LVDS_O	AM335 internal	LVDS0 clock+
X1B63	X_LVDS0_CLK-	LVDS_O	AM335 internal	LVDS0 clock-
X1B64	reference-voltage	REF_O	VMMC_3P3V	LVDS0 reference voltage

Table 30: LVDS Display Interface Signal Location

11.1 Signal Configuration (J12)

J12 selects rising, or falling edge strobe for the LVDS Transmitter at U38 used for the display connectivity of the phyFLEX-AM335x.

J12	Description	Type
1+2	**falling edge strobe used for the LVDS display signals**	0R (0402)
2+3	rising edge strobe used for the LVDS display signals	

Table 31: LVDS Transmitter Signal Configuration J12

11.2 LVDS Display Interface Pixel Mapping

The phyFLEX specification defines the pixel mapping of the LVDS display interface. The pixel mapping equates to the OpenLDI respectively Intel 24.0 or JEIDA standard. Thus you can connect 18-bit as well as 24-bit LVDS displays to the phyFLEX. *Table 32* and *Table 33* show the recommended pixel mapping of the LVDS display.
However since the AM335x LIDD controller supports also the SPWG pixel mapping, this one can be used as well by setting the appropriated configuration bit.

Note:
To be fully compatible to the phyFLEX specification, make sure that the LVDS display you want to use provides the same pin mapping as the phyFLEX (JEIDA respectively OpenLDI). Normally this is only important for 24-bit LVDS displays because due to the organization of the LVDS pixel mapping all common 18-bit LVDS displays should work.

18-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G0	R5	R4	R3	R2	R1	R0
A1	B1	B0	G5	G4	G3	G2	G1
A2	DE	VSYNC	HSYNC	B5	B4	B3	B2
A3	0	0	0	0	0	0	0

Table 32: Pixel Mapping of 18-bit LVDS Display Interface

24-bit LVDS Display

	1	2	3	4	5	6	7
CLK	1	1	0	0	0	1	1
A0	G2	R7	R6	R5	R4	R3	R2
A1	B3	B2	G7	G6	G5	G4	G3
A2	DE	VSYNC	HSYNC	B7	B6	B5	B4
A3	0	B1	B0	G1	G0	R1	R0

Table 33: Pixel Mapping of 24-bit LVDS Display Interface

12 Environment Management IC (EMIC) (U29)

The optional Environment Management IC (EMIC) at U29 gives the possibility to detect, monitor and record particular physical parameter such as current consumption, temperature und voltages. Furthermore the Environment Management IC comes with a PWM output and a tacho input for fan controlling and an I^2C Management bus.

The following table shows the signals of the EMIC available at phyFLEX Connector X1.

Pin #	Signal	ST	Voltage Domain	Description
X1B74	X_PM_SDA	I/O	VMMC_3P3V	EMIC I^2C bus data
X1B75	X_PM_SCL	O	VMMC_3P3V	EMIC I^2C bus clock
X1B79	X_PM_PWM	O		EMIC fan PWM output
X1B80	X_PM_TACHO	I		EMIC fan tacho input

Table 34: Environment Management IC (EMIC) IO Signals

In addition to the signals brought out at the phyFLEX Connector, four temperature sensors and a current sense amplifier are optionally available on the phyFLEX-AM335x. The temperature sensors can be used to monitor the temperature of the Core Power Supply (U24), the RAM (U23), the Controller/PCB (U25), and the Ethernet PHY (U26). The current sense amplifier at U34 serves to monitor the current consumption of the SOM

The table below lists the I^2C addresses of the four temperature sensors, while *Figure 11*and *Figure 12* show the location of the sensors.

Temperature Sensor	Address
RAM (U23)	0x49
Core Power Supply (U24)	0x48
Controller/PCB (U25)	0x4A
Ethernet PHY (U26)	0x4B

Table 35: I^2C addresses of the optional Temperature Sensors

Note:
To avoid any conflicts when connecting external I^2C devices to the EMIC's I^2C bus the addresses of the on-board temperature sensors must be considered.

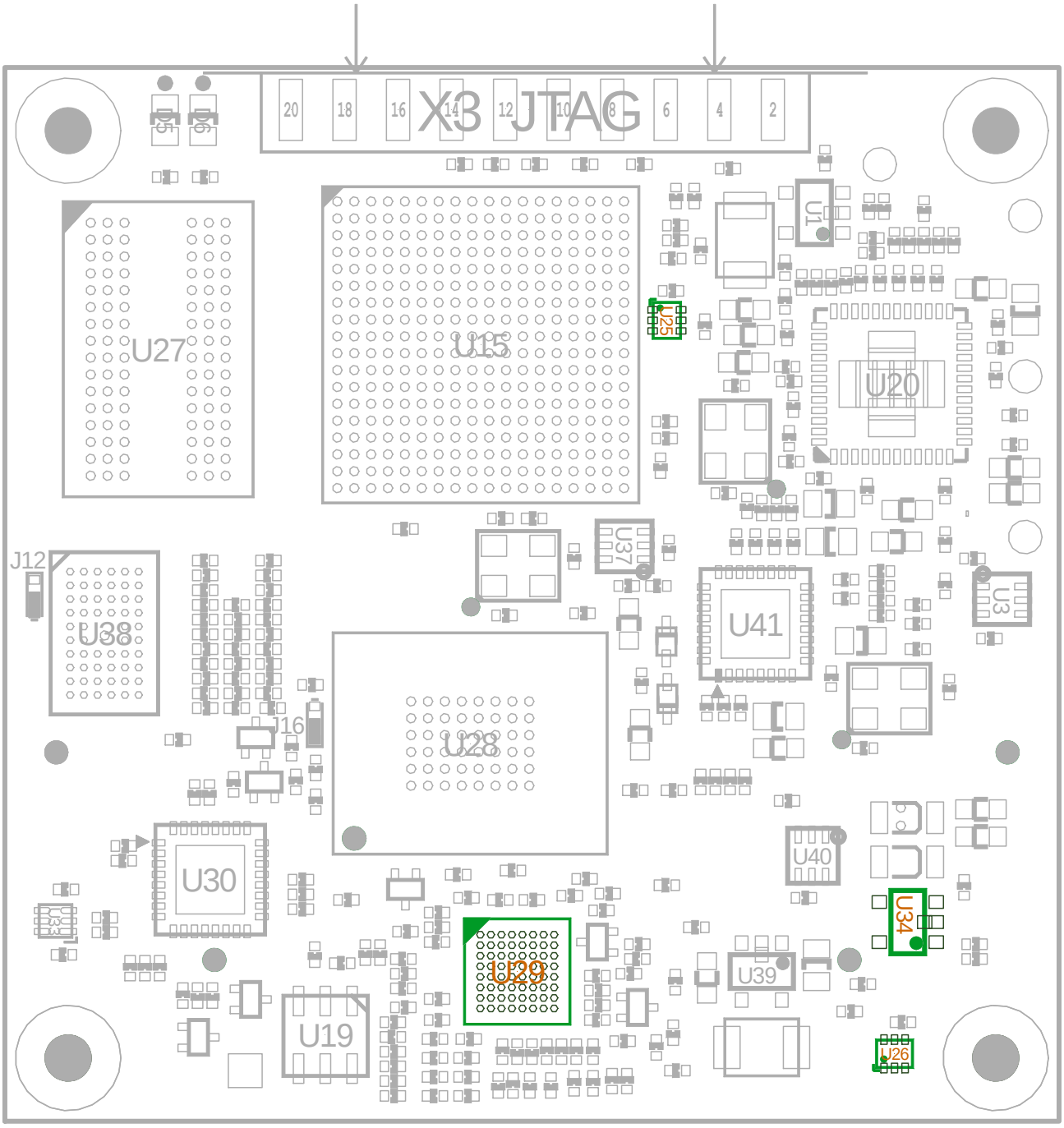


Figure 11: EMIC and supporting Components (top view)

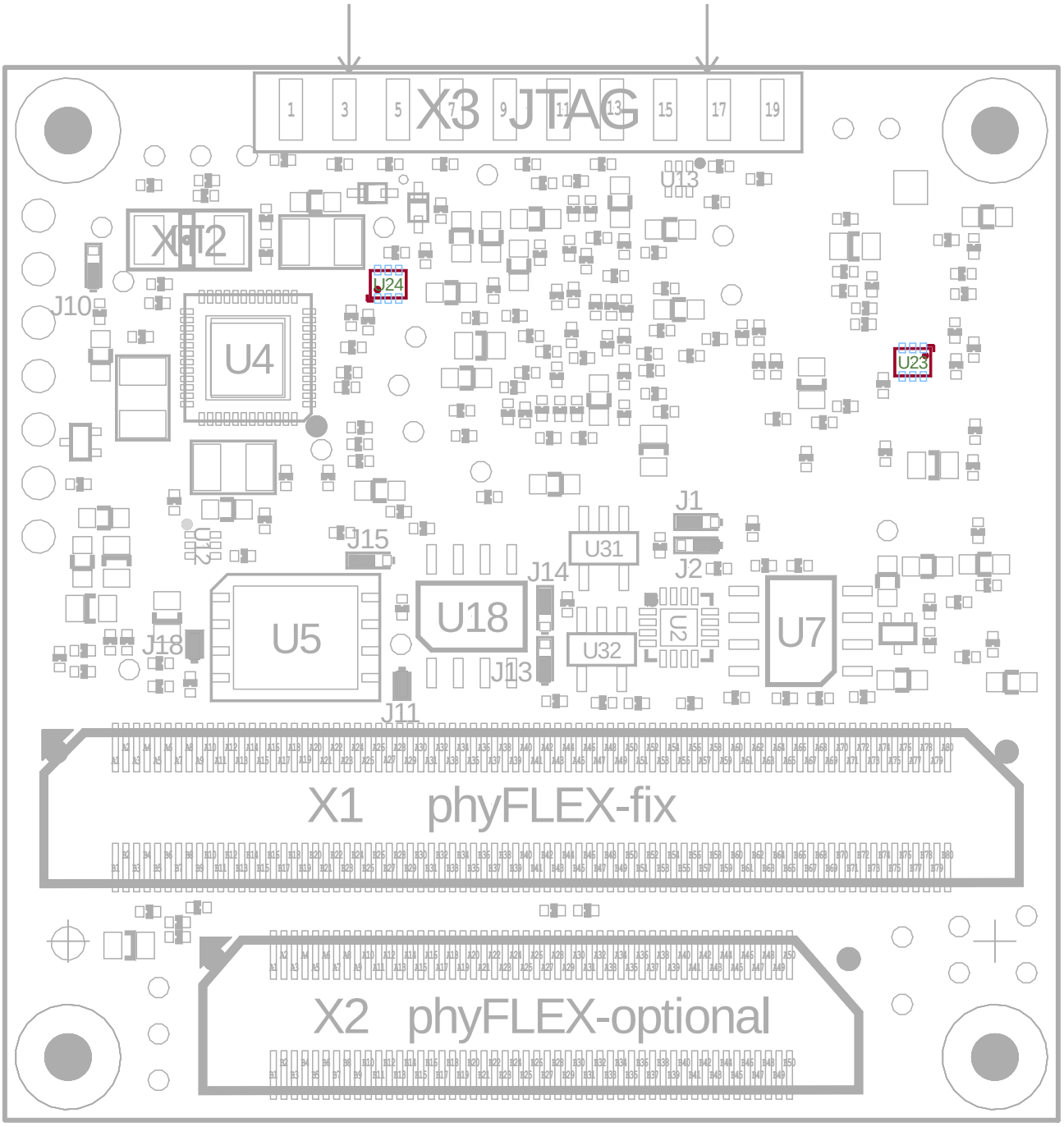


Figure 12: EMIC and supporting Components (bottom view)

13 Technical Specifications

The physical dimensions of the phyFLEX-AM335x are represented in *Figure 13*. The module's profile is max. 10 mm thick, with a maximum component height of 3.0 mm on the bottom (connector) side of the PCB and approximately 5.0 mm on the top (microcontroller) side. The board itself is approximately 1.4 mm thick.

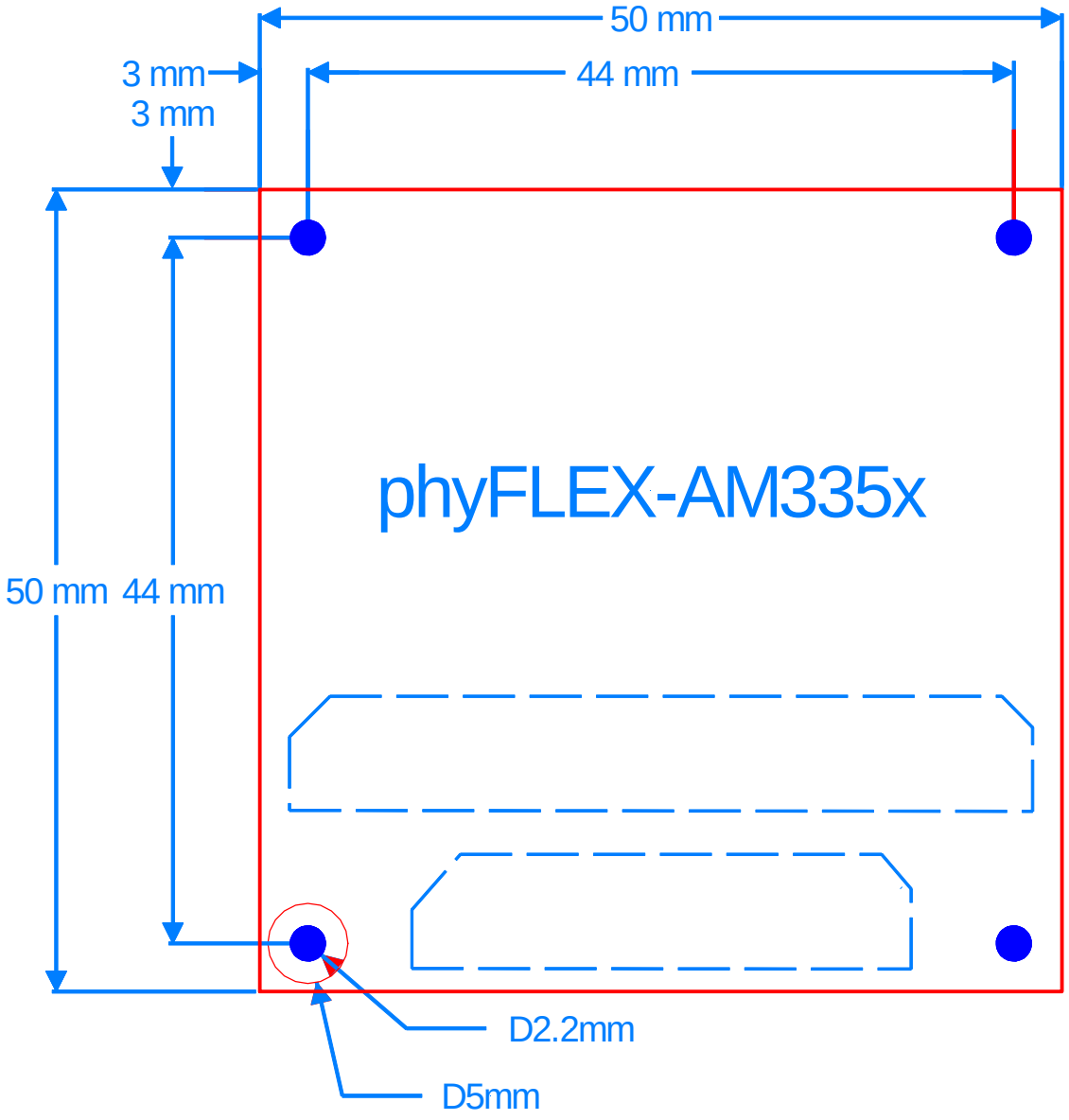


Figure 13: Physical Dimensions (top view)

Note:
To facilitate the integration of the phyFLEX-AM335x into your design, the footprint of the phyFLEX-AM335x is available for download (see *section 14.1*).

Additional specifications:

Dimensions:	50 mm x 50 mm
Weight:	TBD
Storage temperature:	-40°C to +125°C
Operating temperature:	0°C to +70°C (commercial) -40°C to +85°C (industrial)
Humidity:	95% r.F. not condensed
Operating voltage:	VCC 5 V +/- 5%
Power consumption:	TBD

Table 36: Technical Specifications

These specifications describe the standard configuration of the phyFLEX-AM335x as of the printing of this manual.

Connectors on the phyFLEX-AM335x:

Manufacturer	Samtec
	phyFLEX-fix (X1):
Number of pins per contact rows	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	BSH-080-01-L-D-A-K-TR
	phyFLEX-optional (X2):
Number of pins per contact rows	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	BSH-050-01-L-D-A-K-TR

The following list shows the receptacle sockets that correspond to the connectors populating the underside of the phyFLEX—AM335x. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (3 mm) on the bottom side of the phyFLEX must be subtracted.

Connector height 5 mm

Manufacturer	Samtec
Number of pins per contact row	160 pins (2 rows of 80 pins each)
Samtec part number (lead free)	ASP-167037-01 (BTH-080-01-L-D-A-K-TR)
PHYTEC part number (lead free)	VM245
Number of pins per contact row	100 pins (2 rows of 50 pins each)
Samtec part number (lead free)	BTH-050-01-L-D-A-K-TR
PHYTEC part number (lead free)	VM247

Please refer to the corresponding data sheets and mechanical specifications provided by Samtec (*www.samtec.com*).

14 Hints for Integrating and Handling the phyFLEX-AM335x

14.1 Integrating the phyFLEX-AM335x

Besides this hardware manual much information is available to facilitate the integration of the phyFLEX-AM335x into customer applications.

1. the design of the standard phyFLEX Carrier Board can be used as a reference for any customer application
2. many answers to common questions can be found at http://www.phytec.de/de/support/faq/faq-phyFLEX-AM335x.html, or http://www.phytec.eu/europe/support/faq/faq-phyFLEX-AM335x.html
3. the link "Carrier Board" within the category Dimensional Drawing leads to the layout data as shown in *Figure 14*. It is available in different file formats. Use of this data allows to integrate the phyFLEX-AM335x SOM as a single component into your design.
4. different support packages are available to support you in all stages of your embedded development. Please visit http://www.phytec.de/de/support/support-pakete.html, or http://www.phytec.eu/europe/support/support-packages.html, or contact our sales team for more details.

14.2 Handling the phyFLEX-AM335x

- **Modifications on the phyFLEX Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!
If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyFLEX into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyFLEX module. For maximum EMI performance we recommend as a general design rule to connect all GND pins to a solid ground plane. But at least all GND pins neighboring signals which are being used in the application circuitry should be connected to GND.

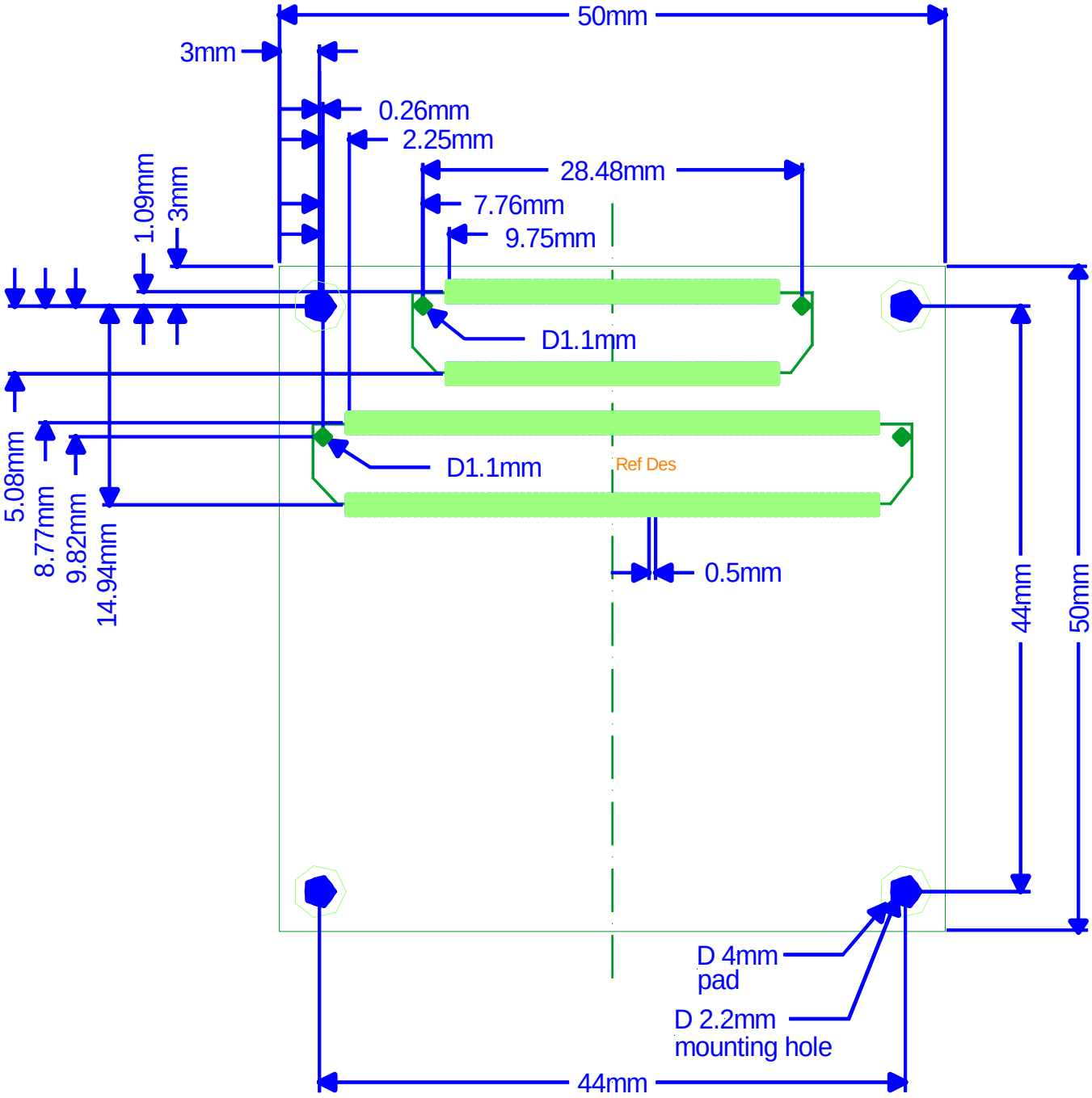


Figure 14: Footprint of the phyFLEX-AM335x

Note:
It must be considered that larger phyFLEX SOMs with a third connector (phyFLEX-flex) are available when designing a custom specific carrier board. If the custom board is meant to also support other phyFLEX SOMs, please download the footprint of the phyFLEX-i.MX 6 at http://www.phytec.de/de/support/faq/faq-phyFLEX-i.MX 6.html (follow the link “Carrier Board” within the category "Dimensional Drawing").

15 The phyFLEX-AM335x on the phyFLEX Carrier Board

PHYTEC phyFLEX Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC System on Module (SOM) modules. phyFLEX Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC System on Module in laboratory environments prior to their use in customer designed applications.

The phyFLEX Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyFLEX-AM335x System on Module. The carrier board design allows easy connection of additional extension boards featuring various functions that support fast and convenient prototyping and software evaluation.

Note:
The following list includes all features of the phyFLEX Carrier Board. Features which are not supported by the phyFLEX-AM335x are in light gray.

The phyFLEX Carrier Board supports the following features for the phyFLEX-AM335x modules:

- Power supply circuits to supply the phyFLEX-AM335x and the peripheral devices of the carrier board
- 12 V Power Supply
- POE+ Power over Ethernet support (25 W)
- Support of all interfaces available at the phyFLEX-fix and phyFLEX-optional Connector
- Support of different power modes of the appropriate phyFLEXs
- Switch to configure the boot order of the AM335x
- Full featured 4 line RS-232 transceiver supporting data rates of up to 1 Mbps, hardware handshake and RS-232 connector
- Second 2 line RS-232 transceiver supporting data rates of up to 1 Mbps
- High integrated and isolated CAN interface
- USB 3.0 Hub with 4 downstream ports available at different connectors (the AM335x supports only USB 2.0)
- USB-OTG interface
- Gbit Ethernet interface
- 10/100 Mbps Ethernet interface
- Support of two I^2C buses from the SOM, available at different connectors on the carrier board (the phyFLEX_AM335x features only one I^2C interface (I2C0))
- Connectivity to two SPI interfaces from the phyFLEX-Module
- Complete audio interface available at four 3.5 mm audio jacks + speaker connector
- DVI interface
- PHYTEC Display Interface (PDI) (LVDS display with separate connectors for data lines and display / backlight supply voltage)

- Circuitry to allow dimming of a backlight
- Touchscreen interface for use of 4 wire resistive touch screens
- Two LVDS camera interfaces compatible to PHYTEC phyCAM-S+ camera standard with I^2C for camera control
- Two Secure Digital Card / Multi Media Card Interfaces (the phyFLEX-AM335x SOM supports only one SD/MM Card Interface)
- PHYTEC Wi-Fi/Bluetooth connector
- DIP-Switch to configure the boot options for the phyFLEX-AM335x module mounted
- RTC with battery supply/backup
- SATA Power and Data connector
- PCIe port
- miniPCIe port
- Five user programmable LEDs
- Pin header connector to connect to 10 GPIOs of the phyFLEX-Module
- JTAG interface for programming and debugging
- Fan Connector
- Environment Management IC (EMIC) for custom specific monitoring of different voltages, currents and temperatures, and for fan control

15.1 Concept of the phyFLEX Carrier Board

The phyFLEX Carrier Board provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyFLEX System on Module. The carrier board design allows easy connection of additional extension boards featuring various functions that support fast and convenient prototyping and software evaluation. The carrier board is compatible with all phyFLEX SOMs.
This modular development platform concept includes the following components:

- the **phyFLEX-AM335x Module** populated with the AM335x processor and all applicable SOM circuitry such as DDR SDRAM, Flash, PHYs, and transceivers to name a few.

- the **phyFLEX Carrier Board** which offers all essential components and connectors for start-up including: a power socket which enables connection to an **external power adapter**, interface connectors such as **DB-9**, **USB** and **Ethernet** allowing for use of the SOM's interfaces with standard cable.

The following sections contain specific information relevant to the operation of the phyFLEX-AM335x mounted on the phyFLEX Carrier Board.

15.2 Overview of the phyFLEX Carrier Board Peripherals

The phyFLEX Carrier Board is depicted in *Figure 15* and *Figure 16*. It is equipped with the components and peripherals listed in *Table* 37, *Table 38*, *Table 39* and *Table 40*. For a more detailed description of each peripheral refer to the appropriate chapter listed in the applicable table. The following figures highlight the location of each peripheral for easy identification.

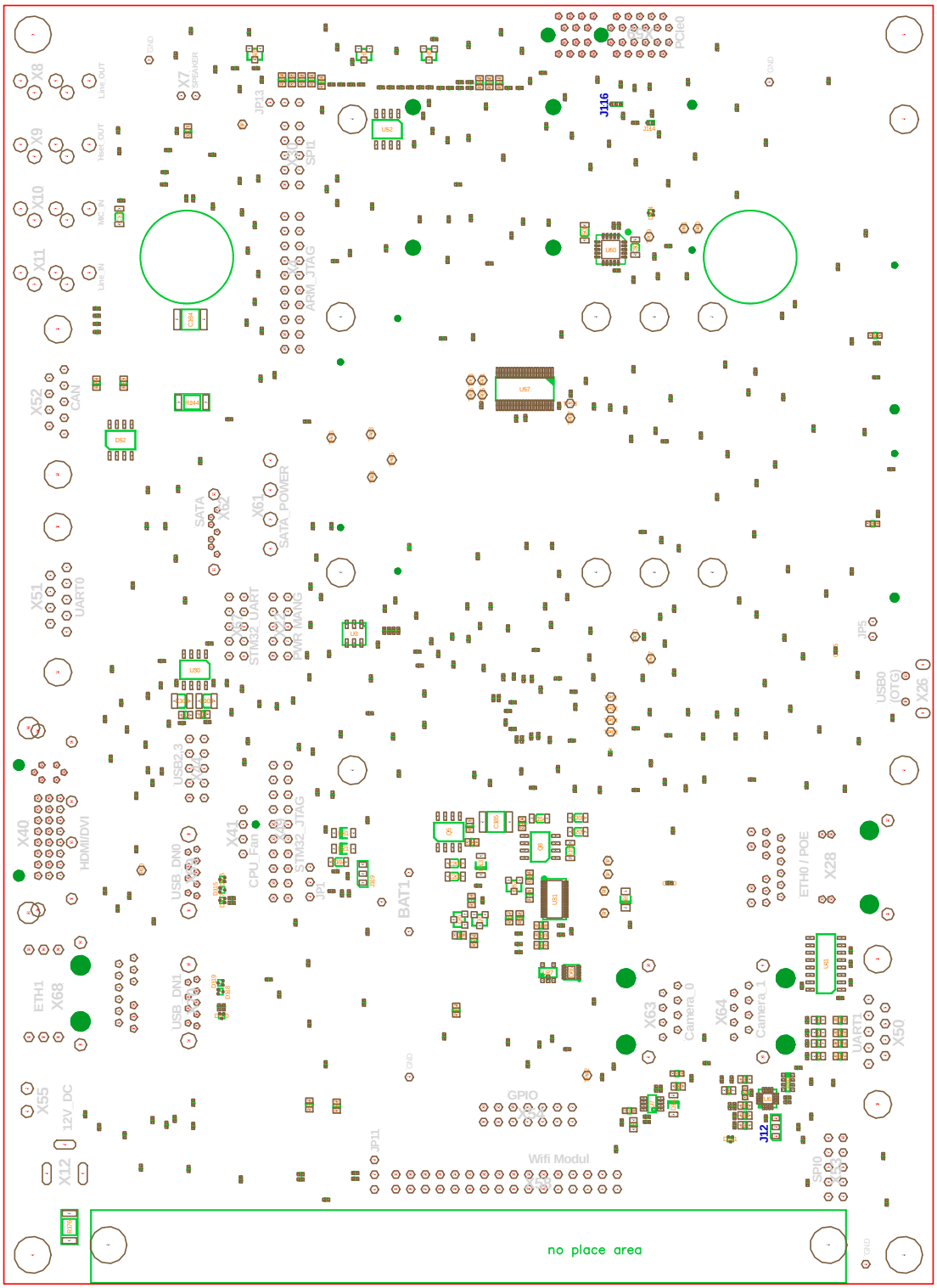


Figure 15: phyFLEX Carrier Board Overview of Connectors, LEDs and Buttons (bottom view)

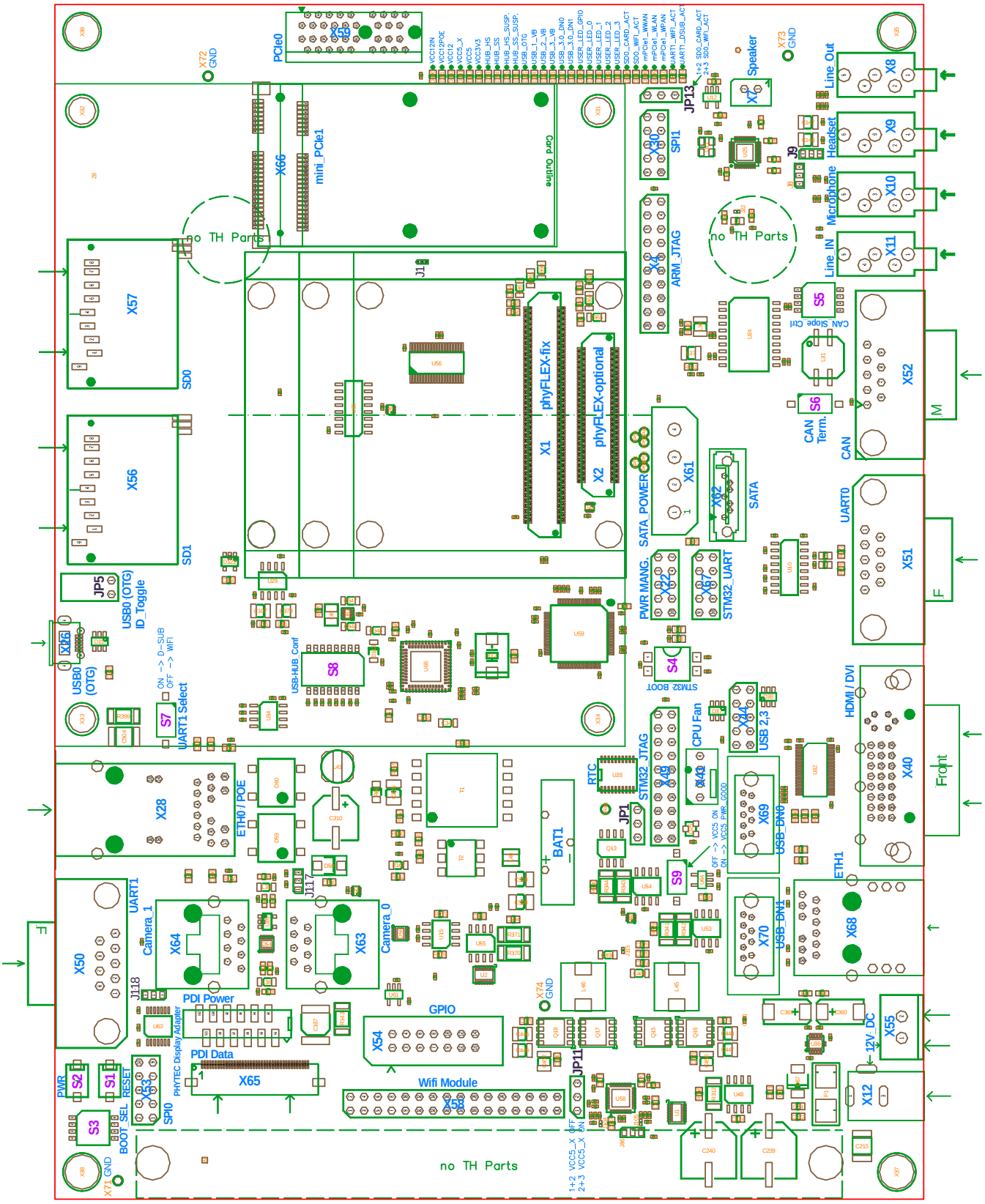


Figure 16: phyFLEX Carrier Board Overview of Connectors, LEDs and Buttons (top view)

Note:
Descriptions printed in light gray in the following tables *Table 37, Table 38, Table 39,* and *Table 40* indicate that the specific feature is not available with the phyFLEX-AM335x.

15.2.1 Connectors and Pin Header

Table 37 lists all available connectors on the phyFLEX Carrier Board. *Figure 16* highlights the location of each connector for easy identification.

Reference Designator	Description	See Section
X1	phyFLEX-fix connector for mounting the phyFLEX-AM335x	*15.3.1*
X2	phyFLEX-optional connector for mounting the phyFLEX-AM335x	*15.3.1*
X4	JTAG (2x10-pin header connector; 2.54 mm pitch)	*15.3.20*
X7	Speaker connector (molex connector; 2.5 mm pitch)	*15.3.9*
X8	Line out connector (3.5 mm stereo jack)	
X9	Headset out connector (3.5 mm stereo jack)	
X10	Microphone in connector (3.5 mm stereo jack)	
X11	Line in connector (3.5 mm stereo jack)	
X12	Wall adapter input power jack to supply main board power (12 V, max. 5 A)	*15.3.2.1*
X22	Power Management signal connector (2x5-pin header connector; 2.54 mm pitch)	
X26	USB OTG connector (USB Micro-AB)	*15.3.7*
X28	Ethernet0/POE connector (RJ45 with speed and link LED)	*15.3.2.2 and 15.3.5*
X30	SPI1 interface (2x5-pin header connector; 2.54 mm pitch)	*15.3.11*
X40	DVI connector	Not supported
X41	CPU fan connector	*15.3.15*
X44	Connector for second and third USB host interface (USB2, USB3) from the SOM (2x5-pin header connector; 2.54 mm pitch)	Not supported
X49	JTAG interface of the Environment Management IC (EMIC) (2x10-pin header connector; 2.54 mm pitch)	*15.3.20*
X50	Serial interface UART1 with handshake signals (DB-9F)	*15.3.3*
X51	Serial interface UART0 without handshake signals (DB-9F)	
X52	CAN interface, DB-9M	*15.3.4*

Table 37: phyFLEX Carrier Board Connectors and Pin Headers

Reference Designator	Description	See Section
X53	SPI0 interface (2x5-pin header connector; 2.54 mm pitch)	15.3.11
X54	GPIO connector (2x7-pin header connector; 2.54 mm pitch)	15.3.12
X55	Alternative power connector (12 V > 5 A) (terminal block; 5.08 mm pitch)	15.3.2.1
X56	Secure Digital/MultiMedia Card slot SD1	Not supported
X57	Secure Digital/MultiMedia Card slot SD0	15.3.14
X58	Wi-Fi/Bluetooth connector (2x16-pin header connector; 2.54 mm pitch)	15.3.16
X59	PCIe connector (PCIe0)	Not supported
X61	SATA power connector	Not supported
X62	SATA data connector	
X63	Camera_0, phyCAM-S+ Connector (RJ45 connector)	Not supported
X64	Camera_1, phyCAM-S+ Connector (RJ45 connector)	
X65	PDI (PHYTEC Display Interface)	15.3.8
X66	Mini PCIe connector (PCIe1)	Not supported
X67	Serial interface of the Environment Management IC (EMIC) (2x5-pin header connector; 2.54 mm pitch)	15.3.22
X68	Ethernet1 (ETH1) connector (RJ45 with speed and link LED)	15.3.5
X69	Downstream USB_DN0 of USB hub U66 (USB 3.0 standard A)	15.3.6
X70	Downstream USB_DN1 of USB hub U66 (USB 3.0 standard A)	

Table 37: phyFLEX Carrier Board Connectors and Pin Headers (continued)

Note:
Ensure that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

15.2.2 Switches

The phyFLEX Carrier Board is populated with some switches which are essential for the operation of the phyFLEX-AM335x module on the carrier board. *Figure 16* shows the location of the switches and push buttons.

Button	Description	See Section
S1	System Reset Button – system reset signal generation	*15.3.18*
S2	Power Button – powering on and off main supply voltages of the carrier board	*15.3.19*
S3	DIP-switch – boot mode selection phyFLEX SOM	*15.3.17*
S4	DIP-switch – boot mode selection EMIC	*15.3.22*
S5	DIP-switch - slope control of the CAN transceiver (U24)	*15.3.4*
S6	DIP-switch – CAN interface terminating	
S7	DIP-switch - UART1 signal routing	*15.3.3* and *15.3.16*
S8	DIP-switch USB Hub Configuration	*15.3.6*
S9	DIP-switch Power ON Handling	*15.3.2*

Table 38: phyFLEX Carrier Board Push Buttons Descriptions

S1 Issues a **system reset** signal. Pressing this button will toggle the X_nPM_RESET_IN pin (X1A72) of the phyFLEX microcontroller LOW, causing the controller to reset.

S2 Issues a **power on/off/wake** event. Pressing this button less than 5 seconds will wake up the phyFLEX-AM335x module and the peripherals on the carrier board, or will turn on the system, if it is powered off. Pressing this button more than 5 seconds will turn off the system without proper shut down of the operating system.

S3 This DIP-switch allows to change the booting device order of the phyFLEX-AM335x.

S4 DIP-switch S4 selects the boot source of the EMIC at U59.

S5 DIP-switch S5 allows two select different modes of operation for the CAN transceiver at U24. To reduce EMI a slope control can be enabled at different speeds.

S6 By using DIP-switch S6 a terminating resistor of 120 Ohm can be connected to the CAN interface.

S7 DIP-switch S7 selects if the TTL signals of UART1 are routed either to the RS-232 transceiver at U11 (thus making UART1 available at DB-9 connector X50 at RS-232 level), or to the Wi-Fi/Bluetooth module connector X58 (at TTL level).

S8 Allows to configure the USB-HUB at U66.

S9 DIP-switch S9 selects whether the voltage VCC5 and VCC3V3 are turned on and off by the PWR_GOOD signal (X_PM_PWR_GOOD, X1A78) of the phyFLEX-AM335x or are permanently switched on.

15.2.3 LEDs

The phyFLEX Carrier Board is populated with numerous LEDs to indicate the status of the various USB-Host interfaces, as well as the different supply voltages. *Figure 16* shows the location of the LEDs. Their function is listed in the table below:

LED	Color	Description	See Section
D91	green	Indicates presence of 12 V input voltage VCC12_POE_X from Ethernet at connector X28	15.3.2
D100	green	Indicates presence of 12 V input voltage VCC12_IN at power connector X12, or X55	
D102	green	12 V supply voltage VCC12 available at the DC-to-DC synchronous buck controller U58 (derived from VCC12_IN or VCC12_POE)	
D101	green	5 V supply voltage VCC5_X for the phyFLEX-AM335x available	
D112	green	5 V supply voltage VCC5 for various peripherals on the phyFLEX Carrier Board present	15.3.2
D111	green	3.3 V supply voltage VCC3V3_X for various peripherals on the phyFLEX Carrier Board available	
D105	green	User LED connected to GPIO10 (P7 from GPIO Expander U2 on the phyFLEX-Am335x)	15.3.13
D97	red	User LED0 (port LED0 from 4-bit LED dimmer at U52)	
D98	yellow	User LED1 (port LED1 from 4-bit LED dimmer at U52)	
D99	yellow	User LED2 (port LED2 from 4-bit LED dimmer at U52)	
D86	green	User LED3(port LED3 from 4-bit LED dimmer at U52)	
D84	green	Indicates presence of VBUS at the first USB Host interface (USB1, USB hub's upstream)	15.3.6
D87	green	VBUS indicator for USB Hub downstream port USB_DN0	
D88	green	VBUS indicator for USB Hub downstream port USB_DN1	
D93	yellow	High-speed indicator LED for USB hub's upstream port connection speed	
D94	yellow	Super-speed indicator LED for USB hub's upstream port connection speed	
D95	yellow	High-speed suspend status indicator LED for USB hub's upstream port	
D96	yellow	Super-speed suspend status indicator LED for USB hub's upstream port	
D85	green	Indicates presence of VBUS at the USB OTG interface (USB0)	15.3.7
D82	green	Indicates presence of VBUS at the module's second USB Host interface (USB2)	Not supported

Table 39: phyFLEX Carrier Board LEDs Descriptions

LED	Color	Description	See Section
D83	green	Indicates presence of VBUS at the module's third USB Host interface (USB3)	Not supported
D106	yellow	SD0 Card connector X57 active	*15.3.14* *15.3.16*
D107	yellow	Wi-Fi/Bluetooth connector X58 active	
D108	yellow	Mini PCIe WWAN status LED	Not supported
D109	yellow	Mini PCIe WLAN status LED	
D110	yellow	Mini PCIe WPAN status LED	
D123	yellow	UART1 signals routed to Wi-Fi/Bluetooth connector X58 (TTL)	*15.3.16*
D124	yellow	UART1 signals available at DB-9F connector X50 (RS-232)	*15.3.3*

Table 39: phyFLEX Carrier Board LEDs Descriptions (continued)

15.2.4 Jumpers

The phyFLEX Carrier Board comes pre-configured with removable jumpers (JP) and solder jumpers (J). The jumpers allow the user flexibility of configuring a limited number of features for development constraint purposes. *Table 40* below lists the jumpers, their default positions, and their functions in each position. *Figure 17* depicts the jumper pad numbering scheme for reference when altering jumper settings on the development board.

Figure 18 provides a detailed view of the phyFLEX Carrier Board jumpers and their default settings. In these diagrams a beveled edge indicates the location of pin 1.

Before making connections to peripheral connectors it is advisable to consult the applicable section in this manual for setting the associated jumpers.

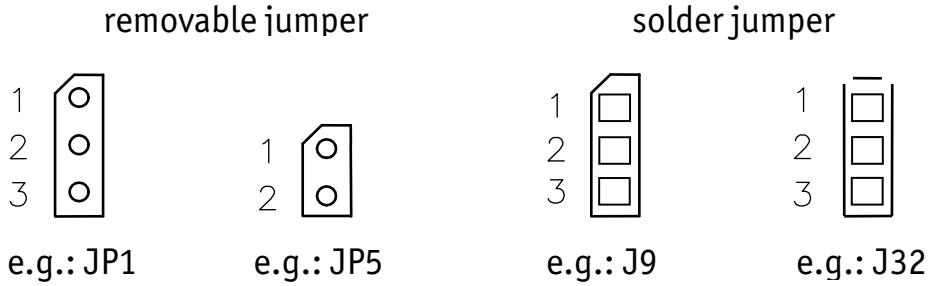


Figure 17: Typical Jumper Numbering Scheme

Table 40 provides a comprehensive list of all carrier board jumpers. The table only provides a concise summary of jumper descriptions. For a detailed description of each jumper see the applicable chapter listing in the right hand column of the table.

If manual modification of the solder jumpers is required please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the board inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

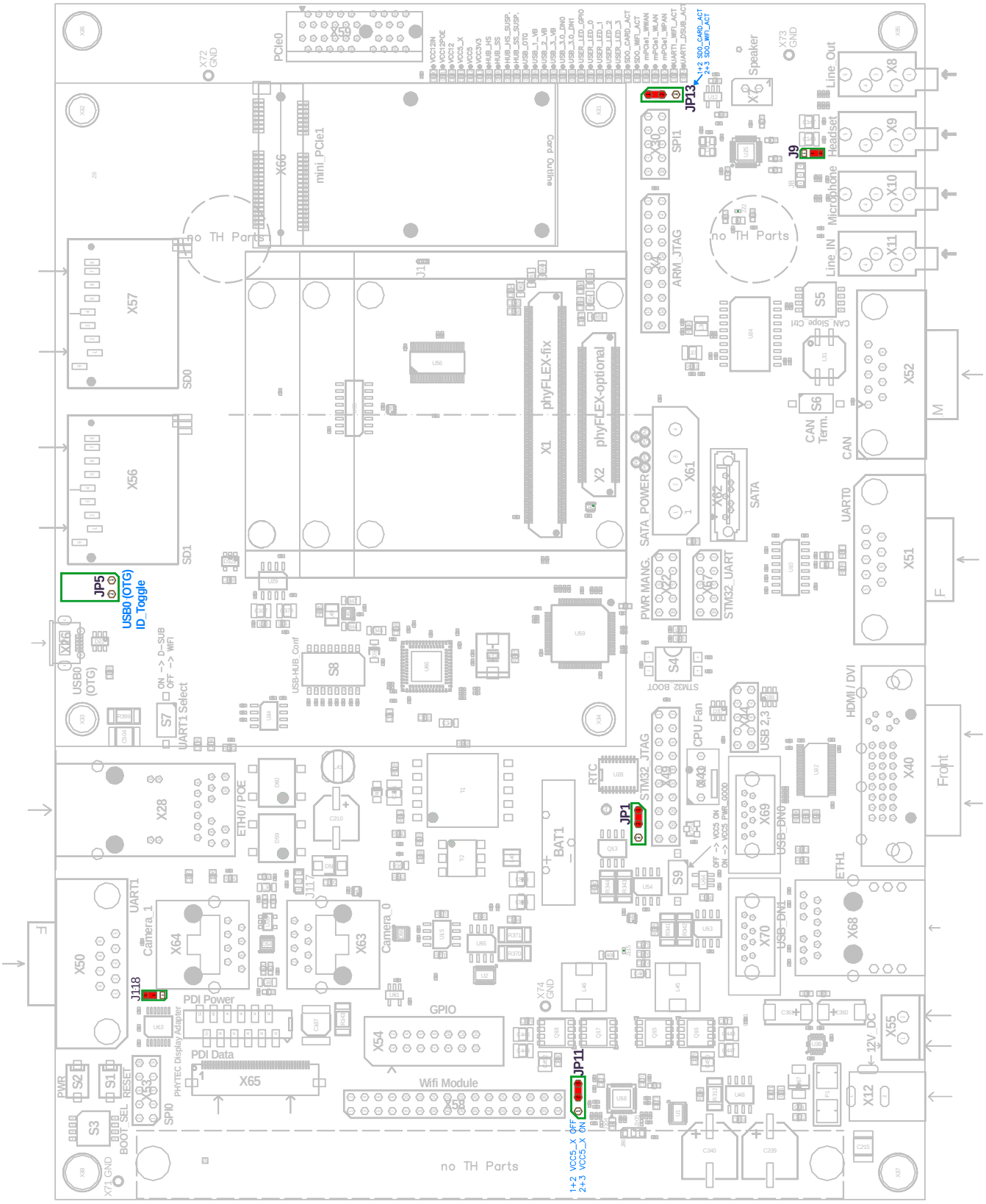


Figure 18: phyFLEX Carrier Board Jumper Locations (top view)

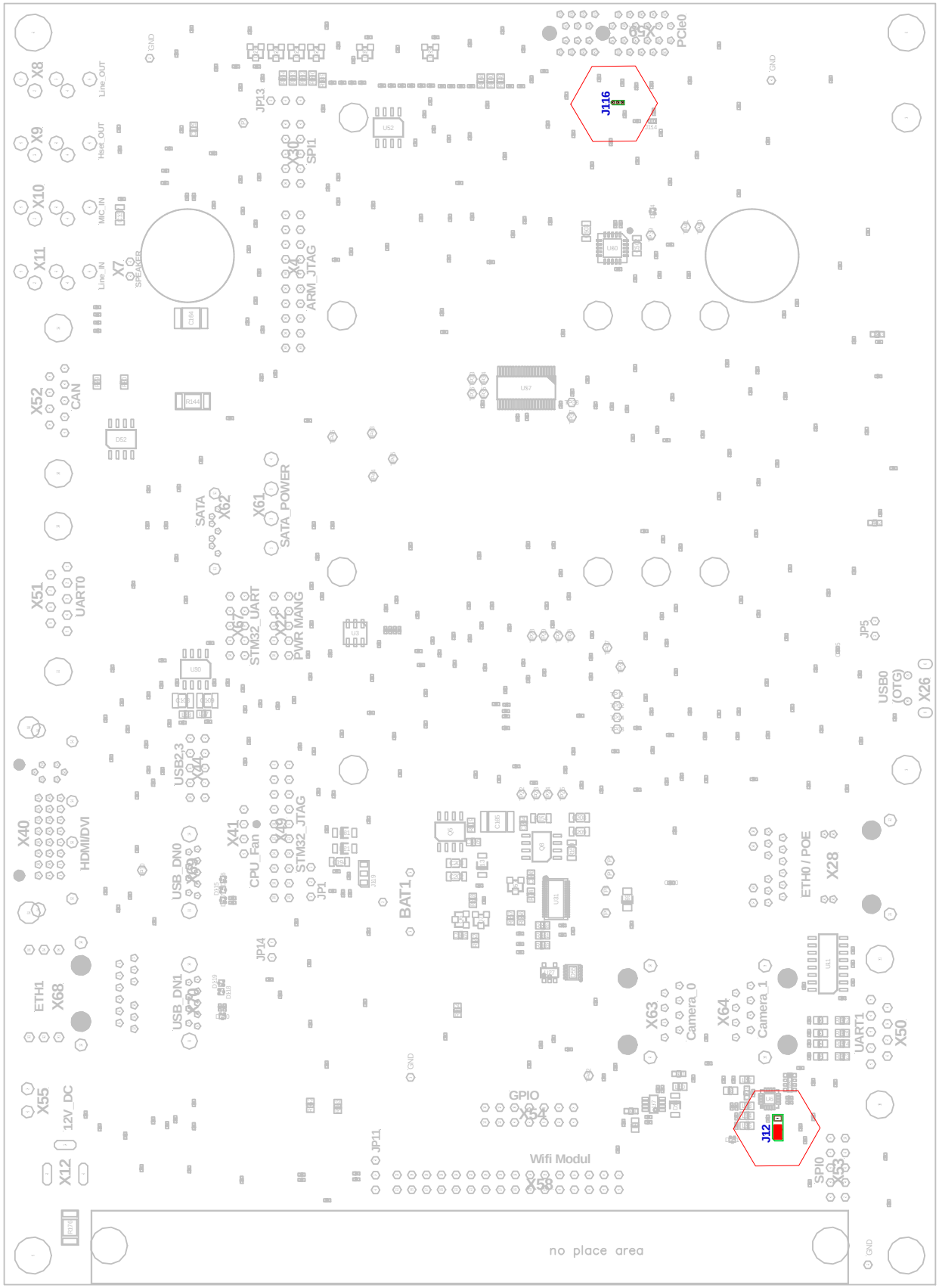


Figure 19: phyFLEX Carrier Board Jumper Locations (bottom view)

The following conventions are used in the Jumper column of jumper *Table 40*.

- J = solder jumper
- JP = removable jumper

Jumper/ Setting	Description	See Section
JP1	Jumper JP1 connects the RTC Interrupt to the Power_ON/Wake/Off Signal or to GPIO5 of the phyFLEX-AM335x (GPIO1_23 of the AM335x)	*15.3.20*
1+2	**RTC interrupt connected to Power_ON/Wake/Off**	
2+3	RTC interrupt connected to GPIO5 (GPIO1_23 of the AM335x)	
JP5	Jumper JP5 forces the USB OTG interface of the phyFLEX-AM335x to function either as host (master), or device (slave)	*15.3.7*
open	**USB0_ID floating, phyFLEX-AM335x in slave mode, or according to the mode configured by software**	
1+2	USB0_ ID connected to GND, phyFLEX-AM335x in host mode	
JP11	Jumper JP11 allows to control the supply voltage VCC5_X of the phyFLEX-AM335x module	*15.3.2*
1+2	SOM supply voltage VCC5_X turned OFF	
2+3	**SOM supply voltage VCC5_X turned ON**	
JP13	Jumper JP13 allows to route the signals of SD0 either to the SD card slot X57, or to the Wi-Fi /Bluetooth connector X58	*15.3.14 and 15.3.16*
1+2	**SD0 routed to the SD card slot X57**	
2+3	SD0 routed to the Wi-Fi /Bluetooth connector X58	
J1	Jumper J1 connects either the global reset signal X_nPM_RESET_OUT to the miniPCIe connector X66, or a reset signal specifically dedicated to the PCIe1 interface (available from some phyFLEX SOMs only)	Not supported
1+2	Global reset signal X_nPM_RESET_OUT connected to miniPCIe connector X66	
2+3	**Specifically dedicated reset signal X_nPCIe1_PERST connected to X66**	
J9	Jumper J9 connects the shield contact of audio jack X9 (headphone out) to either GND, or the HPCOM output driver of the stereo audio codec at U25. Connecting the shield contact to HPCOM allows using the jack detection function of the stereo audio codec.	*15.3.9*
1+2	Shield contact connected to GND, jack detection disabled	
2+3	**Shield contact connected to the HPCOM output driver of the stereo audio codec, jack detection enabled**	

Table 40: phyFLEX Carrier Board Jumper Descriptions

Jumper/ Setting	Description	See Section
J12	Jumper J12 configures the I²C address of the touch screen controller at U6	15.3.8.3
1+2	**Touch Controller (U6) Address: 0x41**	
2+3	Touch Controller (U6) Address: 0x44	
J116	Jumper J116 connects either the global reset signal X_nPM_RESET_OUT to the PCIe connector X59, or a reset signal specifically dedicated to the PCIe0 interface (available from some phyFLEX SOMs only)	Not supported
1+2	Global reset signal X_nPM_RESET_OUT connected to PCIe connector X59	
2+3	**Specifically dedicated reset signal X_nPCIe0_PERST connected to X59**	
J117	Jumper J117 selects the clock signal used for camera interface CAMERA_1. Either a separate ckock signal, or the clock signal of CAMERA_0 can be used. The later configuration is usefull to have both camera interfaces synchronized	Not supported
1+2	**Interface CAMERA_1 operates with dedicated clock signal X_CAMERA1_CLK**	
2+3	Interface CAMERA_1 operates with the same clock signal as interface CAMERA_0	
J118	Jumper J118 allows to switch buffer U63 (relevant for the SPI0 interface at the display data connector) into Three-State Output Mode that reduces supply current	15.3.11
1+2	Three-State Output Mode enabled	
2+3	**normal operation**	

Table 40: phyFLEX Carrier Board Jumper Descriptions (continued)

Note:
Detailed descriptions of the assembled connectors, jumpers and switches can be found in the following chapters.

15.3 Functional Components on the phyFLEX Carrier Board

This section describes the functional components of the phyFLEX Carrier Board supporting the phyFLEX-AM335x. Each subsection details a particular connector/interface and associated jumpers for configuring that interface.

15.3.1 phyFLEX-AM335x SOM Connectivity (X1, X2)

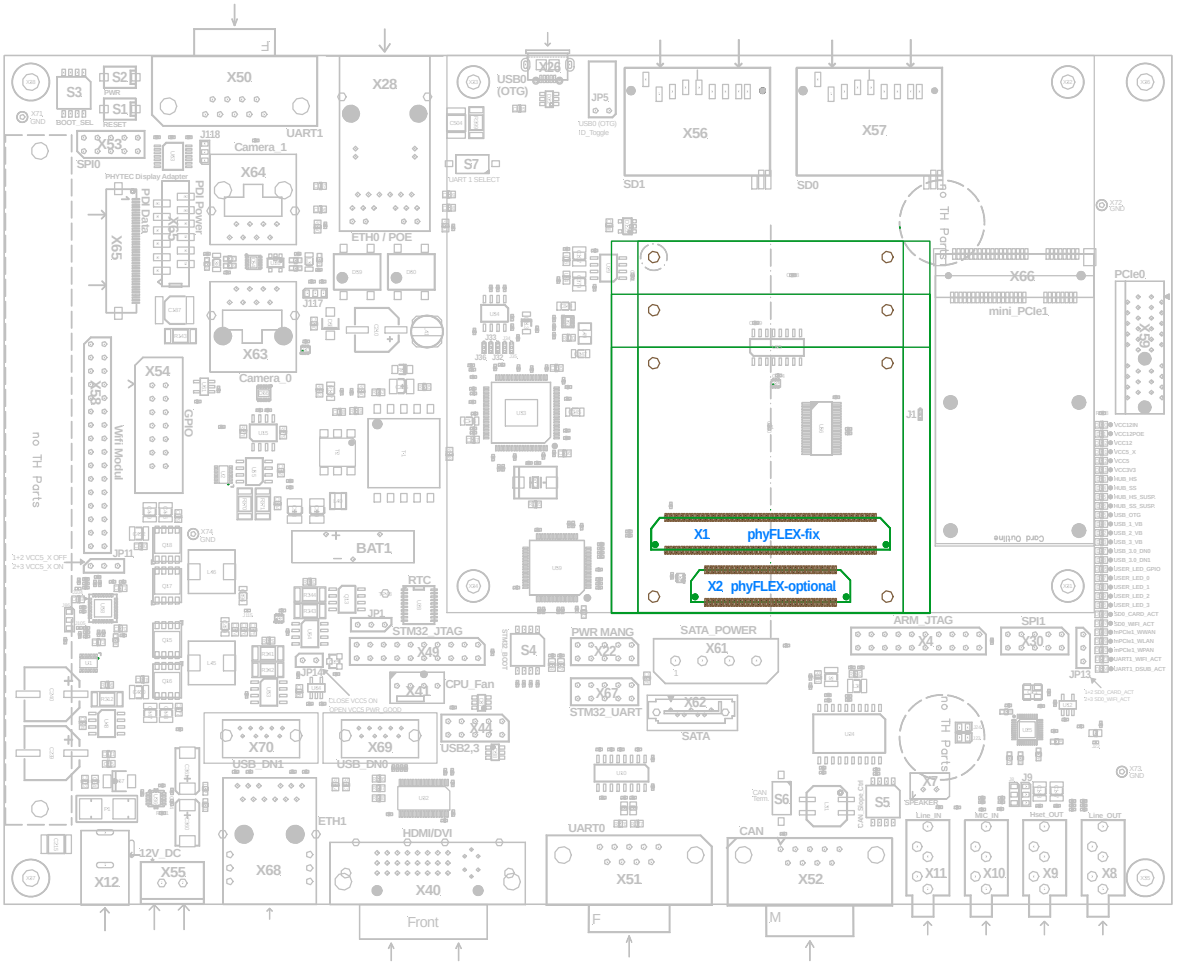


Figure 20: phyFLEX-AM335x SOM Connectivity to the Carrier Board

Connectors X1 and X2 on the carrier board provide the phyFLEX System on Module connectivity. The connector is keyed for proper insertion of the SOM.

Figure 20 above shows the location of connectors X1 and X2, along with the pin numbering scheme as described in *section 2*.

Caution!
Samtec connectors guarantee optimal connection and proper insertion of the phyFLEX-AM335x. Please make sure that the phyFLEX-AM335x is fully plugged into the matting connectors of the carrier board. Otherwise individual signals may have a bad, or no contact.

15.3.2 Power (X12, X55, X28)

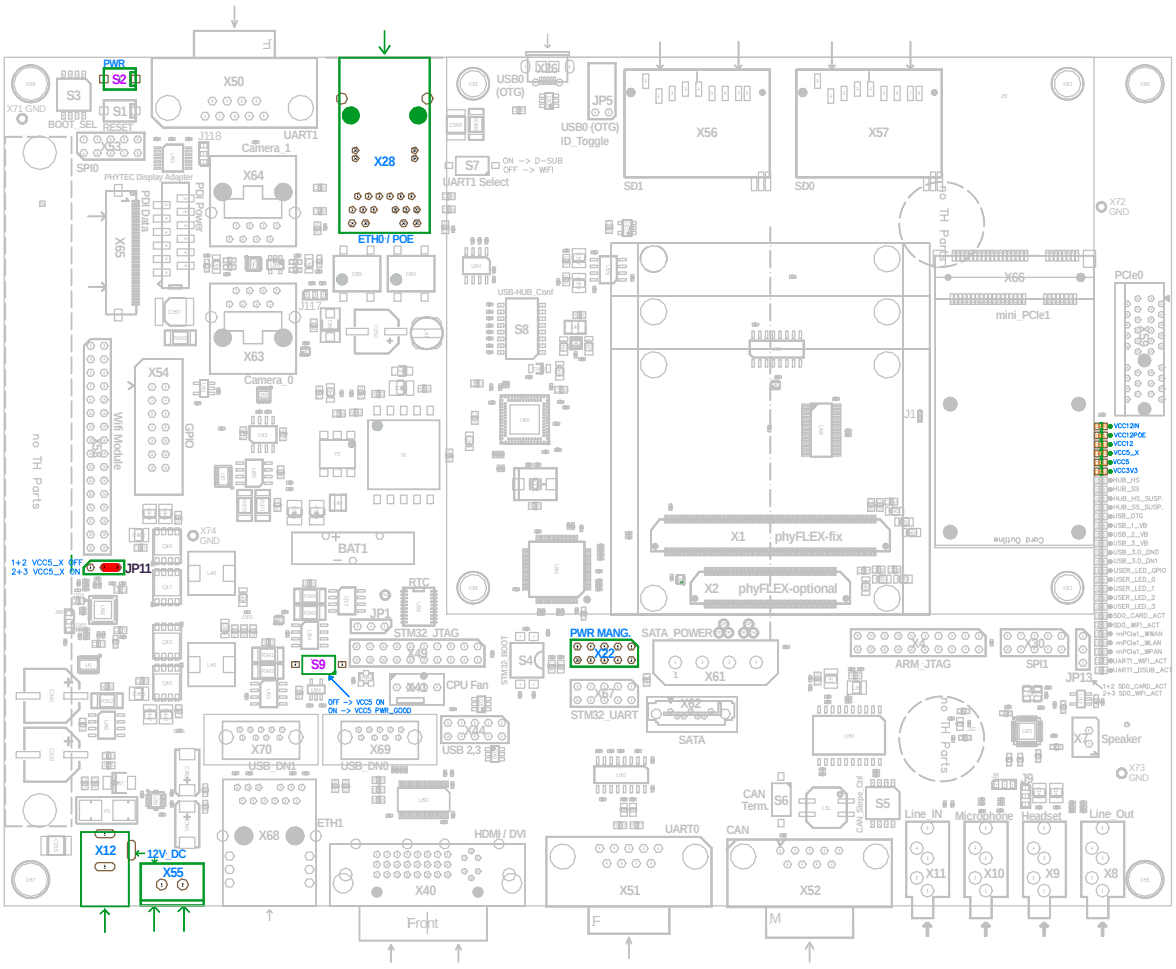


Figure 21: Powering Scheme

The primary input power of the phyFLEX-AM335x Carrier Board comes from either the wall adapter jack X12 (+12 V), or connector X55 (input current > 5 A), or the Power-over-Ethernet circuit (via Ethernet jack X28).

Switching regulators on the carrier board generate seven different voltages to supply the phyFLEX-AM335x and the different components of the carrier board supported by the SOM. The following table lists the voltage domains and their main use.

Voltage domain	Description
VCC12	Supply voltage[1] (VCC5_X, VCC5, VCC3V3, buck converter, PDI interface, PCIe, SATA, CPU fan), resulting from either VCC12_IN, or VCC12_POE
VCC5	Supply voltage[1] (PDI interface, SATA, DVI, CAN, USB)
VCC5_X	Supply voltage phyFLEX SOM
VCC3V3	Supply voltage[1] (PDI, camera, CPU fan, power management, RTC, Wi-Fi/Bluetooth, SD/MMC card interface, UART interface, PCIe)
VCC1V8	Supply voltage Wi-Fi/Bluetooth
VCC1V8_Audio	Supply voltage audio codec
VCC1V5	Supply voltage[1] mini PCIe1 connector X66
VCC1V1	Supply voltage USB Hub U66

Table 41: Voltage Domains on the Carrier Board

Six LEDs on the phyFLEX Carrier Board show the status of the different voltage domains. The assignment of the LEDs to the voltage domains is shown in the following table:

LEDs	Color	Description	
D91	green	VCC12_POE_X –	12 V POE voltage attached to connector X28
D100	green	VCC12_IN –	12 V supply voltage for the phyFLEX Carrier Board attached to connector X12 or X55
D102	green	VCC12 –	12 V supply voltage for DC-to-DC synchronous buck controller and peripherals on the phyFLEX Carrier Board resulting from either VCC12_IN, or VCC12_POE.
D101	green	VCC5_X –	5 V supply voltage for the phyFLEX module
D112	green	VCC5 –	5 V supply voltage for various peripherals on the phyFLEX Carrier Board
D111	green	VCC_3V3_X –	3.3 V supply voltage for peripherals on the phyFLEX Carrier Board

Table 42: Power LEDs

Two jumpers on the phyFLEX Carrier Board allow to enable, or disable single voltage domains. The following table lists the jumpers and the associated voltage domain.

[1]: **Note:** Not all interfaces listed are supported by the phyFLEX-AM335x

Voltage domain	Jumper/ DIP Switch	Description
VCC5, VCC3V3	S9	DIP-switch S9 selects whether the voltage VCC5 and VCC3V3 are turned on and off by the PWR_GOOD signal (X_PM_PWR_GOOD, X1A78) of the phyFLEX-AM335x or are permanently switched on.
	Off	Power_ON connected to high level. VCC5 and VCC3V3 are permanently on
	On	**Power_ON connected to PWR_GOOD. If X_PM_PWR_GOOD (X1A78) is high the voltages VCC5 and VCC3V3 are switched on**
VCC5_X	JP11	Jumper JP11 allows to control the supply voltage VCC5_X of the phyFLEX-AM335x module
	1+2	SOM supply voltage VCC5_X Voltage is turned Off
	2+3	**SOM supply voltage VCC5_X turned On**

Table 43: Power Jumper JP11 and DIP-switch S9

15.3.2.1 Wall Adapter Input (X12)

Caution!
Do not use a laboratory adapter to supply power to the carrier board! Power spikes during power-on could destroy the phyFLEX module mounted on the carrier board! Do not change modules or jumper settings while the carrier board is supplied with power!

Permissible input voltage at X12: 12 V DC regulated (< 5 A).

The required current load capacity of the power supply depends on the specific configuration of the phyFLEX mounted on the carrier board as well as whether optional PCIe boards, USB devices or SATA drives are connected to the carrier board. An adapter with a minimum supply of 2.0 A is recommended.

Caution!
The power supply circuitry on the carrier board is not designed to support all connectable devices at the same time!

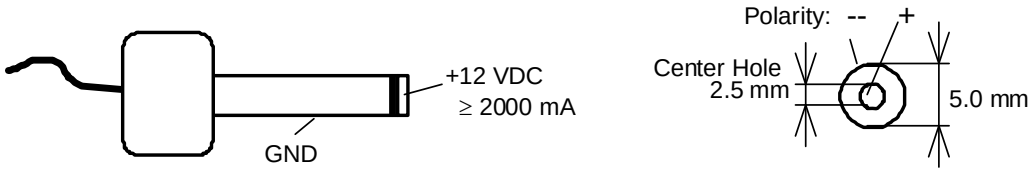


Figure 22: Power Connector corresponding to Wall Adapter Input X12

Note:
If many functions and peripherals of the phyCORE-AM335x kit are used at the same time the power consumption might exceed 60 W (5 A). Wall Adapter Input X12 is not capable to support this. In this case connector X55 must be used. This connector supports a current of up to 16 A..

15.3.2.2 Power over Ethernet Plus (PoE+) (X28)

The Power-over-Ethernet Plus (POE+) circuit provides a method of powering the board via the Ethernet interface. In this configuration the carrier board acts as the Powered Device (PD) while the connecting Ethernet interface acts as the Power Source Equipment (PSE). For applications that require Ethernet connectivity this is an extremely convenient method to also simultaneously provide power. To make use of the PoE circuit a PSE e.g. a PoE enabled router or switch is necessary. LED D91 indicates the availability of the PoE supply voltage.

The PoE+ circuit generates a supply voltage of 12 V, which is feed into the VCC12 branch through an ideal diode.

The IEEE PoE+ standard restricts the maximum amount of power a PSE must provide and therefore a PD can consume. The carrier board PoE+ circuit was designed to provide up to 25 W of power to the board.

The carrier board Ethernet connector X28 supports both PSE sourcing methods of power over the data wires, or power over the spare wires.

Caution!
The PoE+ circuit was designed to provide up to 25 W of power to the board. This is less than the board can potentially consume. Be aware that this limitation could cause board operation to fail if peak power is exceeded due to enabled peripherals. Do not supply the system over Ethernet, if the power consumption expected might exceed 25 W! Do not change modules or jumper settings while the carrier board is supplied with power over the Ethernet!

15.3.2.3 Power Management Connector (X22)

Pin header connector X22 provides the Power Management Signals generated on the phyFLEX-AM335x.

Pin #	Signal Name	Description
1	VCC3V3	3.3 V power supply
2	X_nPM_RESET_OUT	Reset Output
3	X_nPM_RESET_IN	Reset Input
4	X_nPM_ON/WAKEUP/OFF	Power ON/Wake/Off Signal
5	X_PM_SDA	Power Management I²C SDA[1]
6	X_PM_SCL	Power Management I²C SCL[1]
7	NC	not connected
8	X_PM_PWR_GOOD	Power Good Signal
9	NC	not connected
10	GND	Ground

Table 44: Power Management Connector X22

[1]: The function of this signal is not available yet

15.3.2.3.1 Power States

- **RUN** can be entered by pressing using power button S2 less than 5 seconds. Button S2 is connected to the X_nPM_ON/WAKEUP/OFF signal.
- **OFF** can also be entered using power button S2. In this mode we have to make a distinction between two possible of OFF modes. The first is, when the system is shut down by software. In this case, the phyFLEX-AM335x will stop the running processes and shutdown. If button S2 is held for a time longer than 5 seconds, OFF mode will be reached by turning off the phyFLEX-AM335x internal voltages without stopping processes and shutdown.

It is also possible to control state modes from outside the carrier board with the help of the X_nPM_ON/WAKEUP/OFF signal accessible on the Power Management pin header connector X22. To enter the different power states, signal X_nPM_ON/WAKEUP/OFF must be active low for different times as described in the text above.

15.3.3 RS-232 Connectivity (X50, X51)

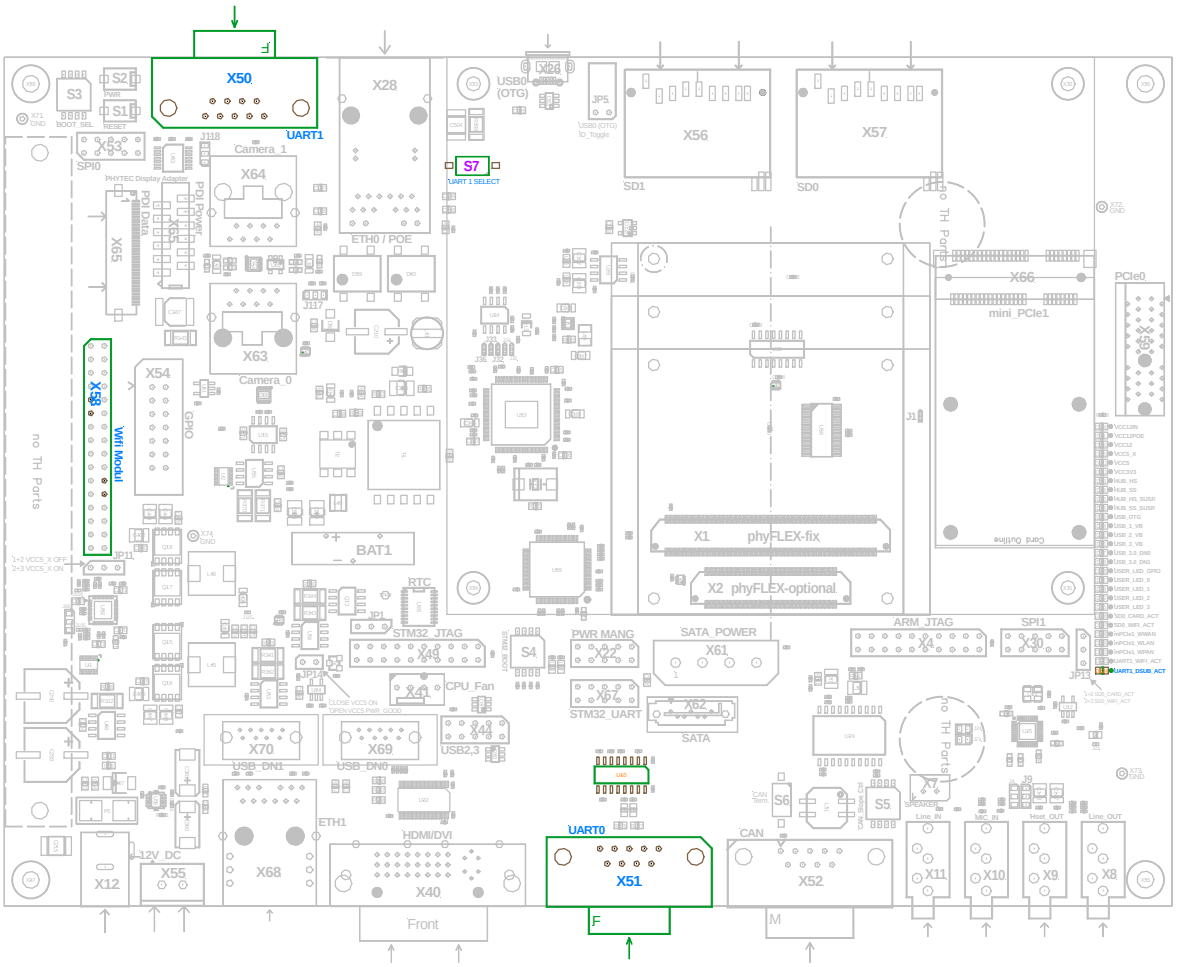


Figure 23: RS-232 Interface Connectors X50 and X51

The phyFLEX Carrier Board supports both UART interfaces (UART0 and UART1) provided by the phyFLEX Module.

Connectors X50 and X51 are DB9 sub-connectors and provide connection interfaces to UART0 (X51) and UART1 (X50) of the phyFLEX-AM335x. Two RS-232 transceivers (U10, U11) on the carrier board convert the TTL level signals from the phyFLEX-AM335x to RS-232 level signals. The serial interface UART1 allows for a 5-wire connection including the signals RTS and CTS for hardware flow control. UART0 provides only signals TX and RX. *Figure 24* and *Figure 25* below show the signal mapping of the RS-232 level signals at connectors X50 and X51.

The RS-232 interface at connector X51 (UART0) is hard-wired and no jumpers must be configured for proper operation.

The TTL signals of UART1 can be routed either to the RS-232 transceiver at U11 and thus providing them at X50 as described above, or they can be routed to the Wi-Fi/Bluetooth connector X58. To use the RS-232 interface UART1 at DB-9F connector X50 DIP-switch S7 must be closed. LED D124 (yellow) indicates that UART1 is available at connector X50.

Please refer to section *15.3.16* for more information on how to use the signals of serial interface UART1 on the Wi-Fi/Bluetooth connector X58 at TTL level.

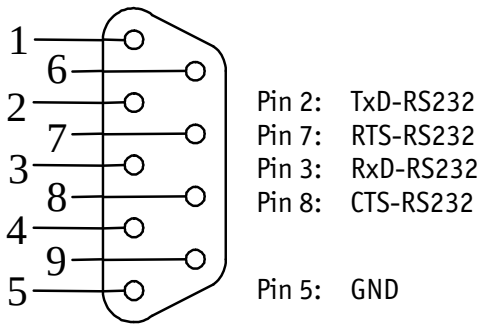


Figure 24: RS-232 Connector X50 Signal Mapping (UART1)

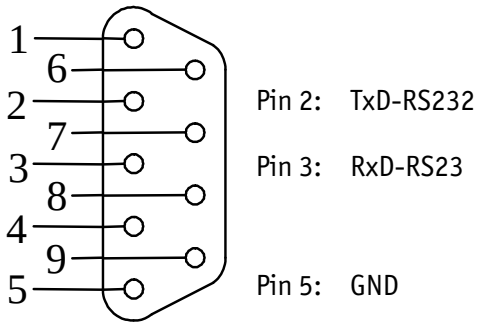


Figure 25: RS-232 Connector X51 Signal Mapping (UART0)

15.3.4 CAN Connectivity (X52)

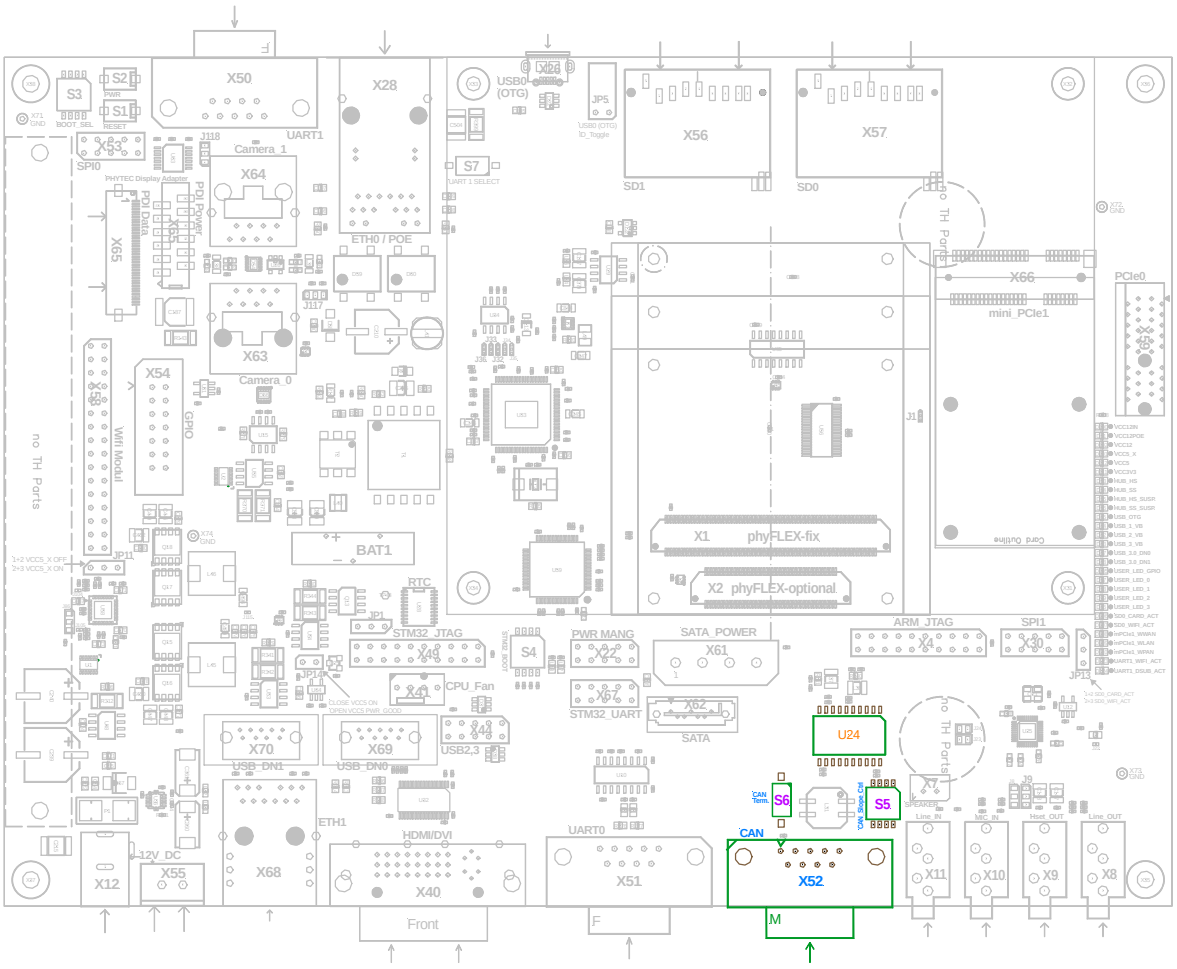


Figure 26: CAN Interface Connector X52

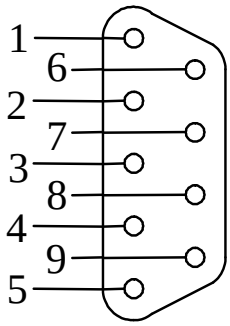
Connector X52 is a SUB-D9M connector and provides connection interfaces to the CAN interface of the AM335x. The TTL level signals from the phyFLEX-AM335x are converted to differential CAN signals by the CAN transceiver at U24. This chip is completely integrated with DC/DC Switching Regulator to generate an isolated 5 V voltage.

The CAN transceiver allows for slope control which can be configured by use of DIP-switch S5. Four different modes of operation can be selected (high-speed and slope control with 3 different speeds). In slope control mode an unshielded twisted pair or a parallel pair of wires can be used as bus lines, while a shielded cable is recommended in high-speed mode to avoid EMI problems. *Table 45* shows the configuration of DIP-switch S5 for the different modes.

Mode of Operation	S5_1	S5_2	S5_3	S5_4
max Slope Control (Lowest Speed / Lowest Emission)	**On**	Off	Off	Off
Slope Control (Low Speed / Low Emission)	Off	**On**	Off	Off
Slope Control (High Speed / High Emission)	Off	Off	**On**	Off
High Speed Mode (Highest Speed / Highest Emission)	Off	Off	Off	**On**

Table 45: phyFLEX Carrier Board DIP Switch S5 Descriptions[1]

DIP-switch S6 can be closed to add a 120 Ohm termination resistor across the CAN data lines if needed.



Pin 6: GND_CAN_ISO
Pin 2: CANL
Pin 7: CANH
Pin 3: GND_CAN_ISO

Figure 27: CAN Connector X52 Signal Mapping

[1]: Default settings are in **bold blue** text

15.3.5 Ethernet Connectivity (X28, X68)

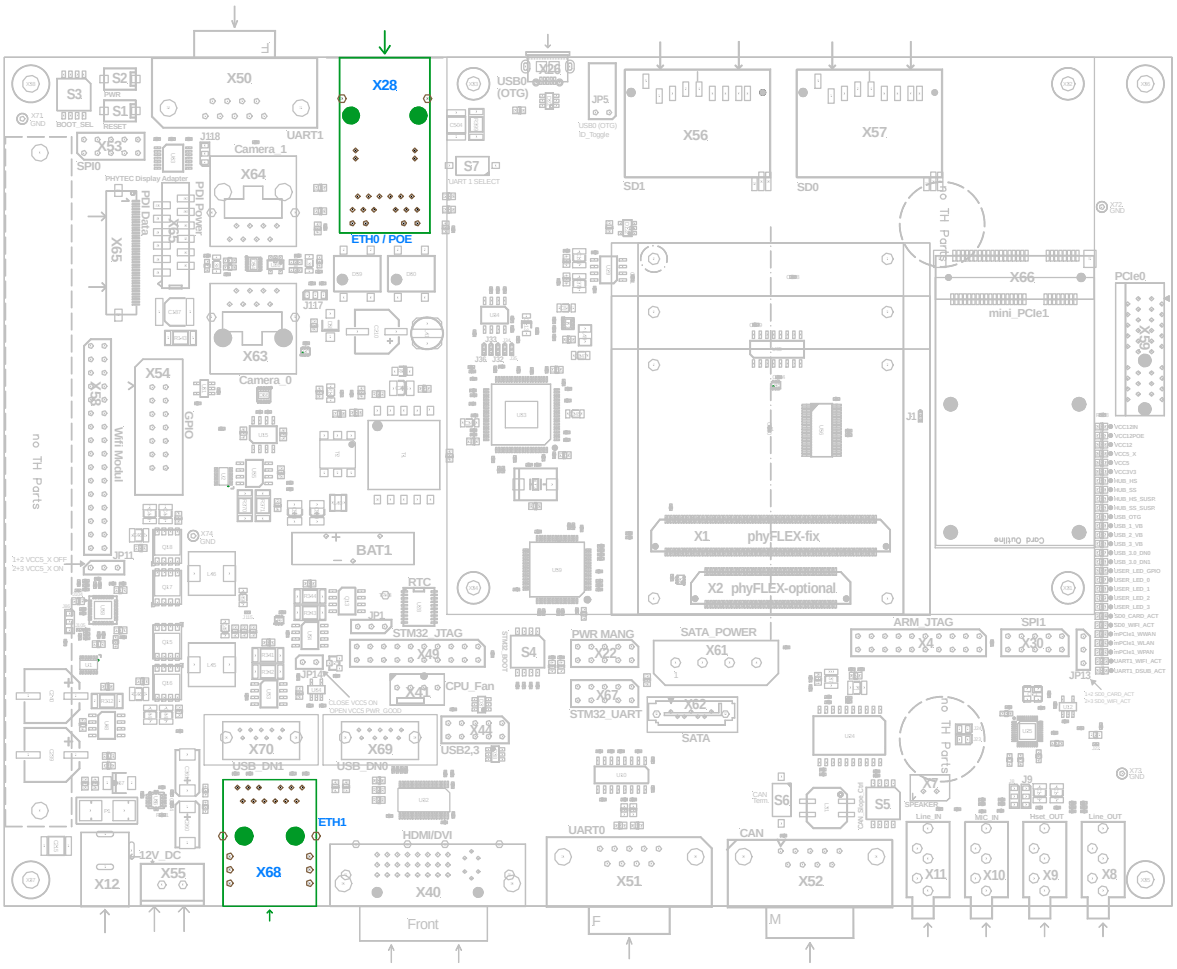


Figure 28: Ethernet Interface at Connector X28, X68

The Ethernet interfaces of the phyFLEX are accessible at the RJ45 connectors X28 and X68 on the carrier board. ETH0 (10/100/1000 Mbit/s) extends to connector X28 while ETH1 (10/100 Mbit/s) is available at X68.

Due to their characteristics these interfaces are hard-wired and can not be configured via jumpers. The LEDs for LINK (green) and SPEED (yellow) indication are integrated in the connectors.

The Gigabit Ethernet interface ETH0 also supports Power over Ethernet (PoE+). Please refer to *section 15.3.2.2* for more information.

15.3.6 USB Host Connectivity (X65, X66, X69, X70, S8)

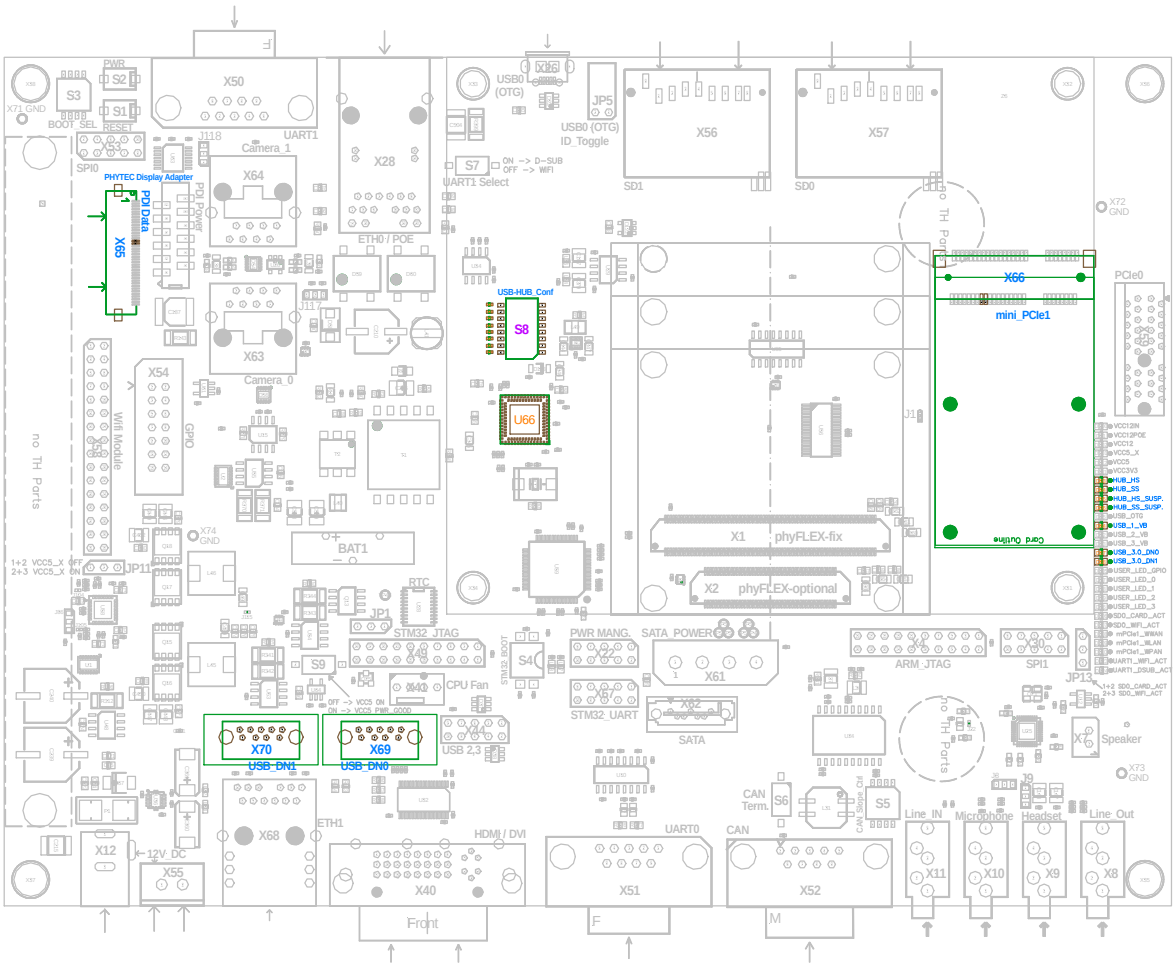


Figure 29: Components supporting the USB Host Interface

The USB host interface (USB1) of the phyFLEX is accessible via the USB hub controller U66 on the carrier board. The controller supports control of input USB devices such as keyboard, mouse or USB key. The USB hub has 4 downstream facing ports. Two ports extend to standard USB A connectors at X69 (USB_DN0) and X70 (USB_DN1). These interfaces are compliant with USB revision 3.0[1]. The remaining ports are accessible at the display data connector X65 and the mini PCIe Connector X66. These two interfaces provide only the data lines D+ and D-. They do not feature a supply line Vbus.

Table 46 shows the distribution of the four downstream facing ports to the different connectors.

[1]: Please note that the USB interfaces of the phyFLEX-AM335x Module are only compliant to USB 2.0. Because of that USB 3.0 devices attached to X69and X70 will not operate at their maximum transmission rate.

USB hub port #	Connector	Connector Type
USB_DN0	X69	USB A (3.0)
USB_DN1	X70	USB A (3.0)
USB_DN2	X65	PDI data connector (40 pin FCC; pins B16 (D+) and B17 (D-))
USB_DN3	X66	Mini PCIe (pins 36 (D-) and D38 (D+))

Table 46: Distribution of the USB Hub's (U66) Ports

LEDs D93 to D96 signal the USB hub's upstream port status. The following table shows the function of the.

LED	Color	Description
D93	**yellow**	High-speed indicator LED for USB hub's upstream port connection speed
D94	**yellow**	Super-speed indicator LED for USB hub's upstream port connection speed
D95	**yellow**	High-speed suspend status indicator LED for USB hub's upstream port
D96	**yellow**	Super-speed suspend status indicator LED for USB hub's upstream port

Table 47: USB Hub's Status LEDs D93 – D96

LEDs D84, D87 and D88 indicate the presence of the VBUS supply voltage.

LED	Color	Description
D84	**green**	USB1_VBUS indicator LED (USB hub's upstream)
D87	**green**	USB30_VBUS_DN0 indicator LED (X69)
D88	**green**	USB30_VBUS_DN1 indicator LED (X70)

Table 48: USB VBUS indicator LEDs

DIP-switch/ Setting	Description
1	Switch 1 of DIP_switch S8 configures the ablity to control power to the downstream ports of the TUSB8040A1 Hub
OFF	**Full Power Management disabled**
ON	Full Power Management enabled
2	Switch 2 of DIP_switch S8 controlls the Interface Mode of the TUSB8040A1 Hub (I²C or SMBus)
OFF	**I²C Mode Selected**
ON	SMBus Selected
3	Switch 3 of DIP_switch S8 controlls the Pullup of the I²C SCL Signal
Off	**I²C SCL Pullup disabled**
On	I²C SCL Pullup enabled
4	Switch 4 of DIP_switch S8 controlls the Pullup of the I²C SDA Signal
Off	**I²C SDA Pullup disabled**
On	I²C SDA Pullup enabled
5	Switch 5 of DIP_switch S8 controlls the Battery Charging option of Downstream Port 0
Off	**Battery Charging Port 0 disabled**
On	Battery Charging Port 0 enabled
6	Switch 6 of DIP_switch S8 controlls the Battery Charging option of Downstream Port 1
Off	**Battery Charging Port 1 disabled**
On	Battery Charging Port 1 enabled
7	Switch 7 of DIP_switch S8 controlls the Battery Charging option of Downstream Port 2
Off	**Battery Charging Port 2 disabled**
Off	Battery Charging Port 2 enabled
8	Switch 8 of DIP_switch S8 controlls the Battery Charging option of Downstream Port 3
Off	**Battery Charging Port 3 disabled**
On	Battery Charging Port 3 enabled

Table 49: USB Hub's Feature Configuration DIP-switch S8

15.3.7 USB OTG Connectivity (X26)

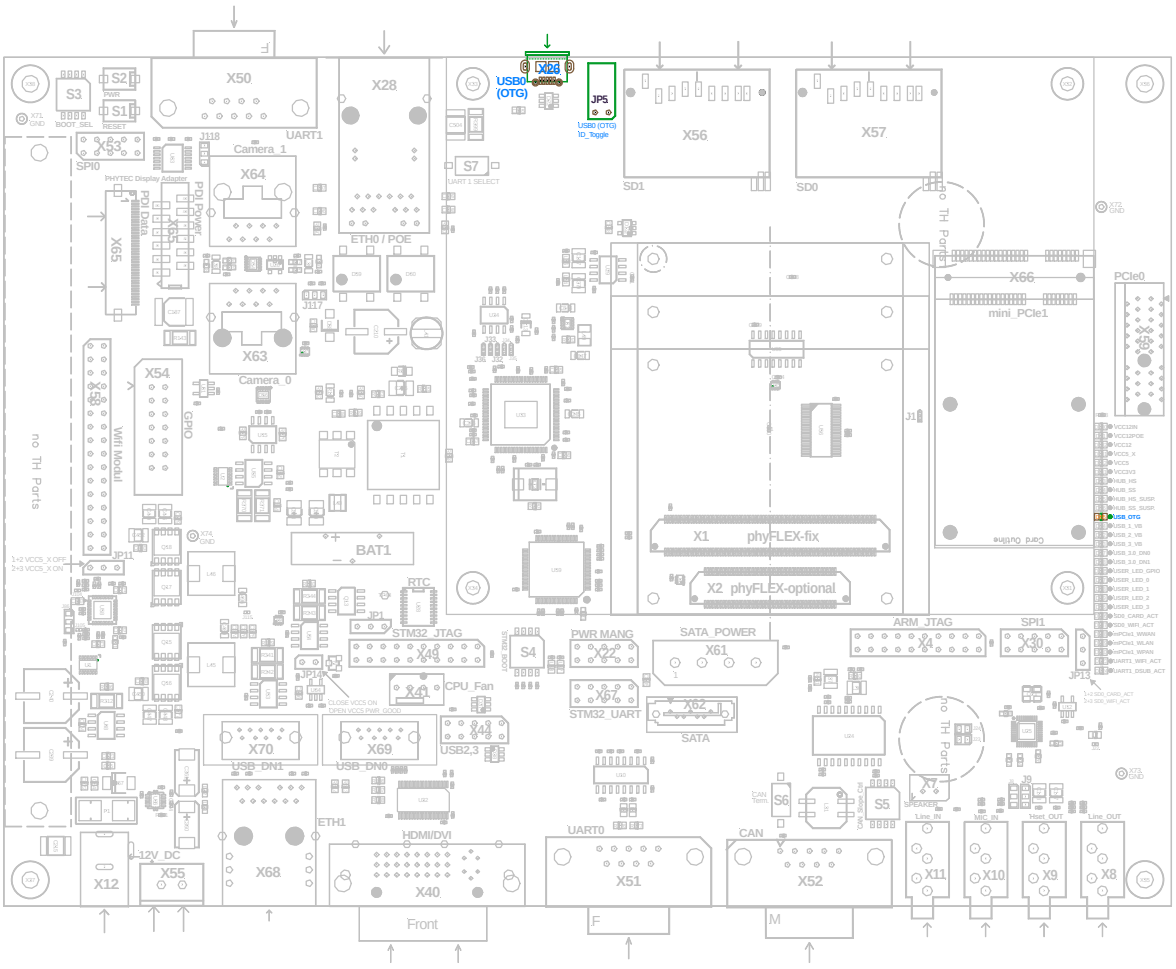


Figure 30: USB OTG Interface at Connector X26

The USB OTG interface of the phyFLEX is accessible at connector X26 (USB Micro-AB) on the carrier board. The phyFLEX-AM335x supports the On-The-Go feature. The Universal Serial Bus On-The-Go is a device capable to initiate the session, control the connection and exchange Host/Peripheral roles between each other. This interface is compliant with USB revision 2.0.

Jumper JP5 configures the OTG operating mode. By default this jumper is open, which leaves the USB_OTG_ID pin floating, and thus configuring the OTG interface as slave. Alternatively this jumper can be closed, connecting USB_OTG_ID to GND, and configuring the OTG interface as host. Typically the configuration of a connecting device as host or slave is done automatically via a USB OTG cable. However, given the limited number of OTG enabled devices in the embedded market this jumper is provided to either simulate an OTG cable, or force the OTG interface into host mode when OTG operation is not required.

LED D85 (green) signals VBUS power output.

15.3.8 Display / Touch Connectivity (X65)

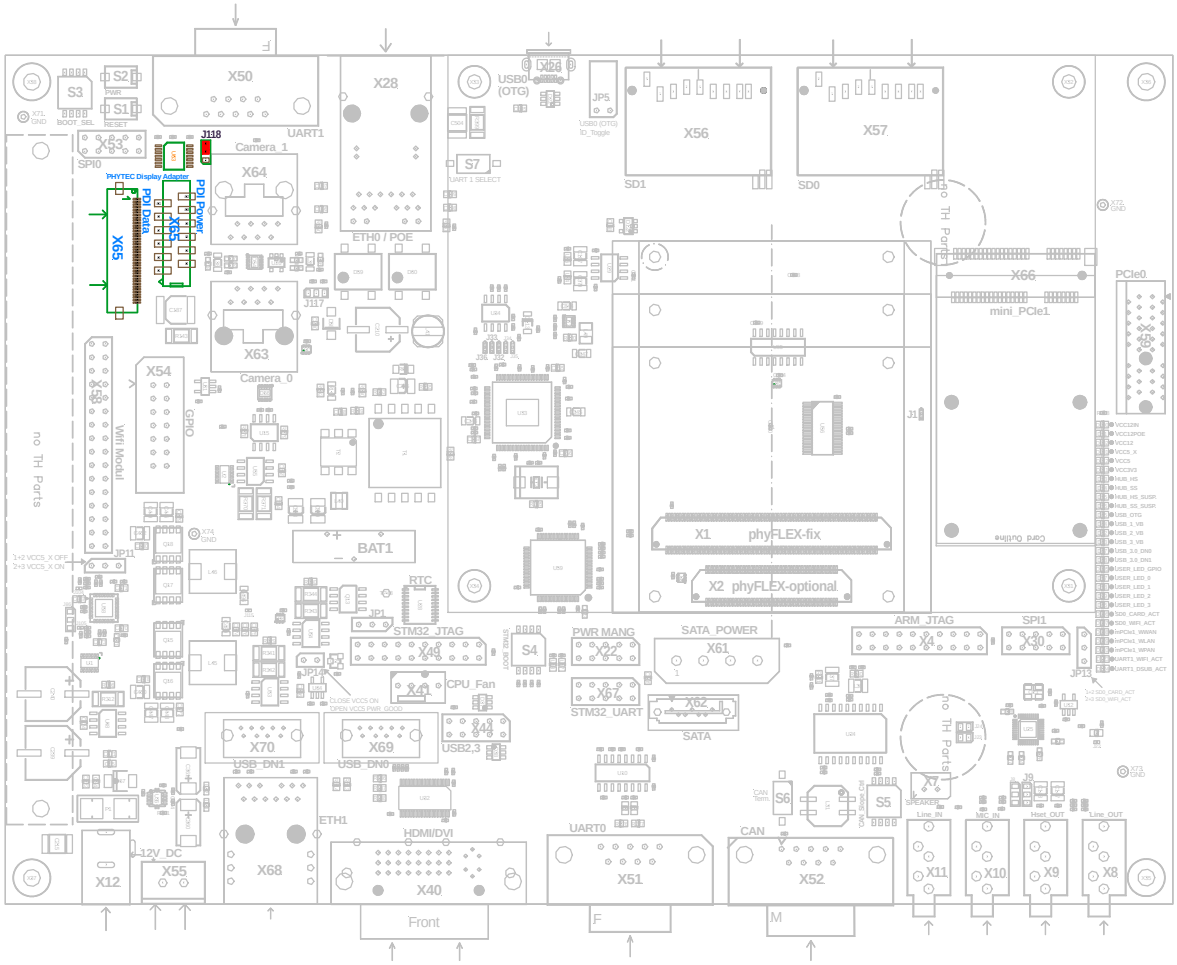


Figure 31: PHYTEC Display Interface (PDI) at Connector X65

The various performance classes of the phyFLEX family allow to attach a large number of different displays varying in resolution, signal level, type of the backlight, pinout, etc. In order not to limit the range of displays connectable to the phyFLEX, the phyFLEX carrier board has no special display connector suitable only for a small number of displays. The new concept intends the use of an adapter board (e.g. PHYTEC's LCD display adapters LCD-014, LCD-017 and LCD-018) to attach a special display, or display family to the phyFLEX. A new PHYTEC Display-Interface (PDI) was defined to connect the adapter board to the phyFLEX Carrier Board. It consists of two universal connectors which provide the connectivity for the display adapter. They allow easy adaption also to any customer display. One connector (40 pin FCC connector 0.5 mm pitch) at X65 is intend for connecting all data signals to the display adapter. It combines various interface signals like LVDS, USB, I^2C, etc. required to hook up a display. The second connector of the PDI (AMP microMatch 8-338069-2) at X65 provides all supply voltages needed to supply the display and a backlight, and the brightness control.

The following sections contain specific information on each connector.

15.3.8.1 Display Data Connector (X65)

PDI data connector X65 provides display data from the serial LVDS display interface of the phyFLEX- AM335x (see *section 11*).

In addition other useful interfaces such as USB, I²C, etc. are available at PDI data connector X65. *Table 51* lists all miscellaneous signals and gives detailed explanations. The following table shows the pin-out of the PDI's display data connectors at X65.

The display data connector at X65 is 40 pin FCC connector with 0.5 mm pitch.

Pin #	Signal name	ST	SL	Description
B1	SPI0_CLK_LCD	O	3.3 V	SPI 0 clock
B2	SPI0_MISO_LCD	I/O	3.3 V	SPI 0 master data in; slave data out
B3	SPI0_MOSI_LCD	O/I	3.3 V	SPI 0 master data out; slave data in
B4	SPI0_CS1_LCD	O	3.3 V	SPI 0 chip select display
B5	X_GPIO6	I	3.3 V	Display interrupt input (connects to GPIO3_7 of the AM335x)
B6	VCC3V3	O	3.3 V	Power supply display[1]
B7	X_I2C0_SCL	I/O	3.3 V	I²C clock signal
B8	X_I2C0_SDA	I/O	3.3 V	I²C data signal
B9	GND	-	-	Ground
B10	X_LVDS_DISP_BL_PWM	O	3.3 V	PWM brightness output
B11	VCC3V3	O	3.3 V	Logic supply voltage[1]
B12	X_nPM_ON/WAKEUP/OFF	I	3.3 V	Power on/off Button
B13	X_nLVDS_DISP_ENA	O	3.3 V	Display enable signal
B14	X_HW-Introspection	I/O	3.3 V	Hardware Introspection Interface **for internal use only**
B15	GND	-	-	Ground
B16	USB_DP_DN2	I/O	3.3 V	USB_DN2 data +
B17	USB_DM_DN2	I/O	3.3 V	USB_DN2 data -
B18	GND	-	-	Ground
B19	X_LVDS_L0-	O	3.3 V	LVDS data channel 0 negative output
B20	X_LVDS_L0+	O	3.3 V	LVDS data channel 0 positive output
B21	GND	-	-	Ground
B22	X_LVDS_L1-	O	3.3 V	LVDS data channel 1 negative output
B23	X_LVDS_L1+	O	3.3 V	LVDS data channel 1 positive output
B24	GND	-	-	Ground

Table 50: PDI Data Connector X65 Signal Description

[1]: Provided to supply any logic on the display adapter. Max. draw 100 mA

B25	X_LVDS_L2-	O	3.3 V	LVDS data channel 2 negative output
B26	X_LVDS_L2+	O	3.3 V	LVDS data channel 2 positive output
B27	GND	-	-	Ground
B28	X_LVDS_L3-	O	3.3 V	LVDS data channel 3 negative output
B29	X_LVDS_L3+	O	3.3 V	LVDS data channel 3 positive output
B30	GND	-	-	Ground
B31	X_LVDS_CLK-	O	3.3 V	LVDS clock channel negative output
B32	X_LVDS_CLK+	O	3.3 V	LVDS clock channel positive output
B33	GND	-	-	Ground
B34	TS_X+	I/O	3.3 V	Touch
B35	TS_X-	I/O	3.3 V	Touch
B36	TS_Y+	I/O	3.3 V	Touch
B37	TS_Y-	I/O	3.3 V	Touch
B38	NC	-	-	not connected
B39	GND	-	-	Ground
B40	LS_ANA	I	3.3 V	Light sensor analog input

Table 50: PDI Data Connector X65 Signal Description (continued)

The table below shows the auxiliary interfaces at display data connector X65.

Signal	Description
USBDN2	USB host interface derived form port 2 of the USB hub at U66. Suitable for optional features e.g. front USB.
I2C0	I²C interface for optional EEPROM, or other I²C devices
SPI0	SPI interface to connect optional SPI slave
1-WIRE	Hardware Introspection Interface **For internal use only**
X_nPM_ON/WAKEUP/OFF	Power on/off signal to allow for an ON/OFF switch on a front panel. It connects to the PWRON input of the CMIC on the phyFLEX-AM335x and to the power management connector X22
X_nLVDS_DISP_ENA	Can be used to enable, or disable the display, or to shutdown the backlight.
X_LVDS_DISP_BL_PWM	PWM output to control the brightness of a display´s backlight (0%=dark, 100%=bright).
LS_ANA	Analog light sensor input. The analog light sensor input at pin 40 extends to an 8-bit A/D converter (U7) which is connected to the I2C0 Bus at address 0x64. To get the maximum adjustment range the output voltage of an applicable light sensor should range from 0 V to VRef (VCC3V3).

Table 51: Auxiliary Interfaces at PDI Data Connector X65

All signals of the SPI interface at the display data connector are routed through a buffer at U63. Jumper J118 allows to switch the buffer into Three-State Output Mode that reduces supply current (refer to *section 15.3.11* for more information).

15.3.8.2 Display Power Connector (X65)

The display power connector X65 (AMP microMatch 8-188275-2) provides all supply voltages needed to supply the display and a backlight.

Pin #	Signal name	ST	SL	Description
A1	GND	-		Ground
A2	VCC3V3	O	3.3 V	3.3 V power supply display
A3	GND	-		Ground
A4	VCC5	O	5 V	5V power supply display
A5	GND	-		Ground
A6	VCC5	O	5 V	5 V power supply display
A7	GND	-		Ground
A8	VCC5	O	5 V	5 V power supply display
A9	GND	-		Ground
A10	X_LVDS_DISP_BL_PWM	O	3.3 V	PWM brightness output
A11	VCC12	O	+12 V	Backlight power supply
A12	VCC12	O	+12 V	Backlight power supply

Table 52: PDI Power Connector X65 Signal Description

15.3.8.3 Touch Screen Connectivity

As many smaller applications need a touch screen as user interface, provisions are made to connect 4- wire resistive touch screens to the PDI data connector X65 (pins B34 - B37, refer to *Table 50*). The signals from the touch screen panel are processed by a touch panel controller at U6. The touch panel controller is connected to I^2C bus I2C0 at address 0x41.

By changing jumper J12 (on the backside of the CB (see *Figure 19*) the address can be set to 0x44 if needed (refer to *Table 40*).

An additional interrupt output is connected to X_GPIO0 of the phyFLEX-AM335x (X1A54 on the phyFLEX-fix Connector; GPIO1_24 of the AM335x).

15.3.9 Audio Interface (X7, X8, X9, X10, X11)

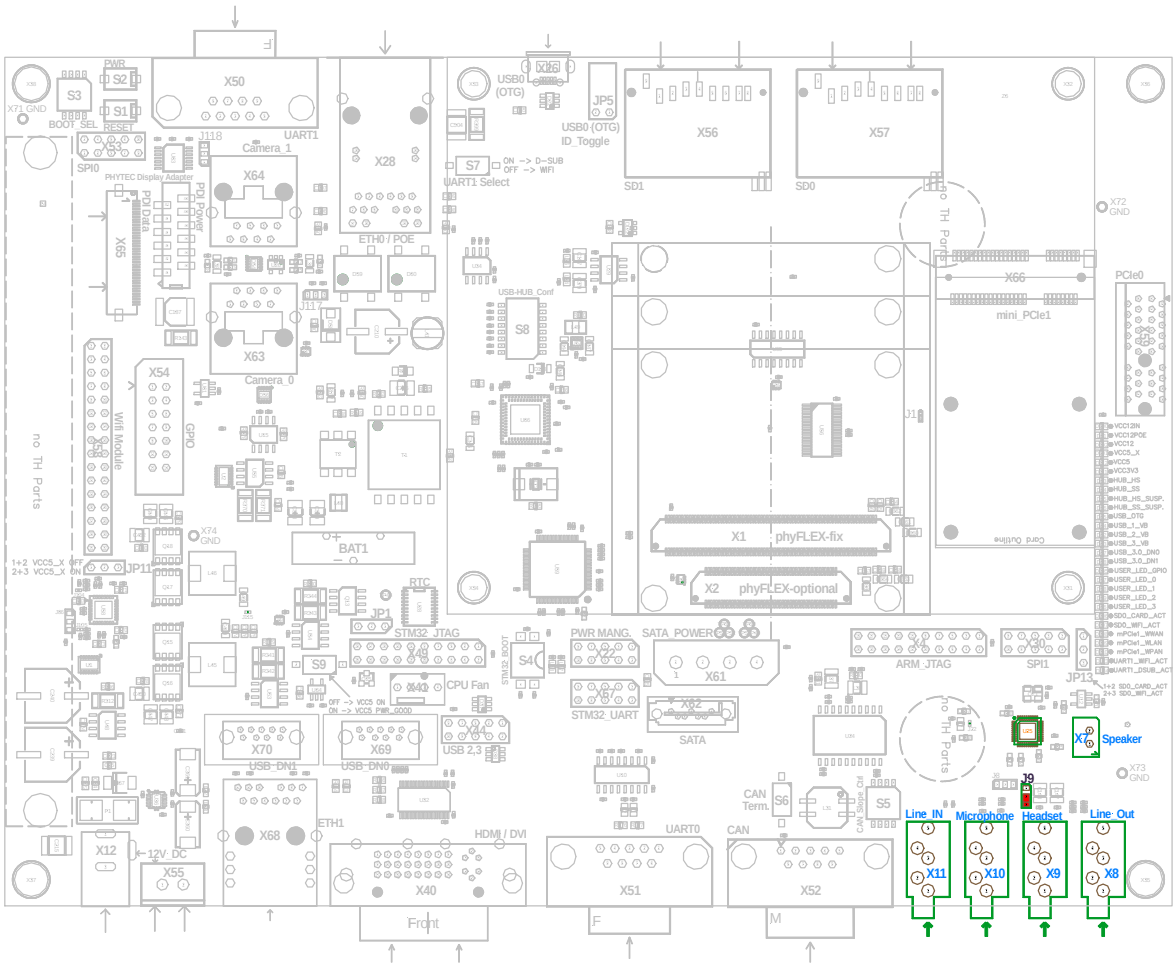


Figure 32: Audio Interface at Connectors X7, X8, X9, X10, X11

The audio interface provides a method of exploring the phyFLEX-AM335x I²S capabilities. The phyFLEX Carrier Board is populated with a low-power stereo audio codec with integrated mono class-d amplifier at U25. It provides a High Performance Audio DAC and ADC with sample rates from 8 kHz to 96 kHz. It supports a stereo line input, stereo microphone input, stereo line output, stereo headphone output and direct speaker output.

The audio codec is interfaced to the phyFLEX-AM335x via I²S interface for audio data and the I2C0 interface for codec configuration (I²C address 0x18). Audio devices can be connected to 3.5 mm audio jacks at X8, X9, X10 and X11. A detailed list of applicable connectors is presented below. The pin header connector at X7 allows for direct connection of a Mono Class-D 1W BTL 8 Ohm Speaker.

Audio Outputs:

X8 – Line Output
X9 – Headset Output
X7 – Speaker Output

Audio Inputs:

X10 – Microphone In
X11 – Line In

Please refer to the audio codec´s reference manual for additional information regarding the special interface specification.

The audio codec´s master clock of 19.2 MHz will be generated at OZ1 on the carrier board.

The microphone input (X10) and the headset output (X9) allow jack detection. The jack detection of the microphone input is hardwired, while jack detection of the headset output can be disabled by jumper J9. In default position (2+3) jumper J9 connects the shield contact of audio jack X9 (headset out) to the HPCOM output driver of the stereo audio codec at U25. In this configuration jack detection is enabled. Connecting the shield contact to GND (J9 at 1+2) disables the jack detection function.

15.3.10 I²C Connectivity

The carrier board provides two I²C buses (I2C0 and I2C1). These are available at different connectors on the phyFLEX Carrier Board.

Note:

The phyFLEX-AM335x SOM supports I2C0 only. I2C1 is not supported.

The following table provides a list of the connectors and pins with I²C connectivity.

Connector	Location
Camera interface X63	pin 4 (I2C_SDA_CAMERA); pin 5 (I2C_SCL_CAMERA) derived from I2C1 (Not supported with phyFLEX-AM335x)
Camera interface X64	pin 4 (I2C_SDA_CAMERA); pin 5 (I2C_SCL_CAMERA) derived from I2C1 (Not supported with phyFLEX-AM335x)
Display data connector X65	pin B8 (X_I2C0_SDA); pin B7 (X_I2C0_SCL)

Table 53: I²C Connectivity

To avoid any conflicts when connecting external I²C devices to the phyFLEX Carrier Board the addresses of the on-board I²C devices must be considered, as well as the addresses of the I²C devices on the phyFLEX-AM335x. On the carrier board only I2C0 is used for the different devices. Some of the addresses can be configured by jumper. *Table 54* lists the addresses already in use. The table shows only the default address. Please refer to *section 15.2.4* and *8.5* for alternative address settings.

Device (on the phyFELX-AM335x)	Address used I2C0 (7 MSB)	Jumper
EEPROM (U18)	0x52	J13, J14
GPIO Expander (U2)	0x19	J1, J2
PMIC (U4)	0x2D 0x12 (SmartReflex)	
EMIC (U29)	tbd.	
Device (on the Carrier Board)	**Address used I2C0 (7 MSB)**	**Jumper**
RTC (U28)	0x51	
A/D converter (U7)	0x64	
Touch screen controller (U6)	0x41 (Switchable to 0x44)	J12
Audio Controller (U25)	0x18	
LED dimmer (U52)	0x62	

Table 54: I2C0 Addresses in Use

15.3.11 SPI Connectivity (X30, X53)

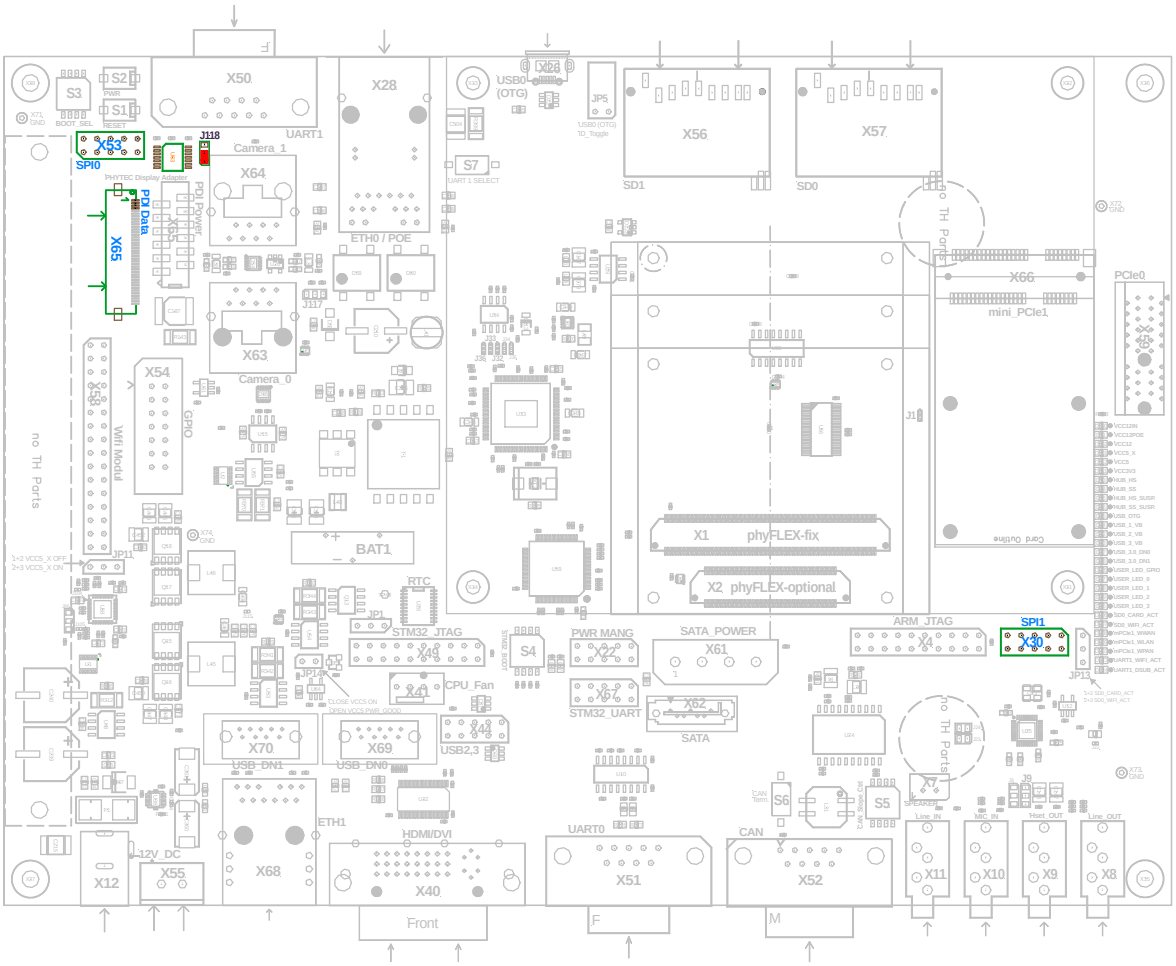


Figure 33: Audio Interface at Connectors X7, X8, X9, X10, X11

The carrier board supports connectivity to both SPI Interfaces of the phyFLEX module.

The SPI0 interface is available at the SPI0 pin header connector X53, and display data connector X65. All signals of the SPI interface at the display data connector are routed through a buffer at U63. Jumper J118 allows to switch the buffer into Three-State Output Mode that reduces supply current (see *Table 57*).

The phyFLEX-AM335x supports the 3 slave select signals X_SPI0_CSBOOT, X_SPI_CS0, and X_SPI0_CS1 (refer to *section 8.6*). X_SPI0_CSBOOT is reserved to address the SPI Flash on the module and is not available on the carrier board.

Connector	Location
PDI data connector X65	pin B1 (SPI0_CLK_LCD); pin B2 (SPI0_MISO_LCD); pin B3 (SPI0_MOSI_LCD); pin B4 (SPI0_CS1_LCD), all signals routed through buffer U63
SPI0 pin header connector X53	see *Table 56*

Table 55: SPI0 Connector Selection

Pin	ST	SL	Description
1	NC	-	not connected
2	NC	-	not connected
3	NC	-	not connected
4	O	3.3 V	X_SPI0_CS0 (GPIO1_19 of AM335x)
5	O	3.3 V	X_SPI0_CS1 (SPI0_CS1 of AM335x)
6	I	3.3 V	X_SPI0_MISO
7	O	3.3 V	X_SPI0_MOSI
8	O	3.3 V	X_SPI0_CLK
9	-	GND	Ground
10	O	3.3 V	VREF_SPI0

Table 56: SPI0 Pin Header X53 Pinout

SPI Buffer Mode of Operation	J118
Three-State Output Mode enabled	1 + 2
normal operation	**2 + 3**

Table 57: SPI Buffer U63 Mode of Operation

The second SPI1 interface is available with two chip selects at pin header connector X30.

Pin	ST	SL	Description
1	NC	-	not connected
2	NC	-	not connected
3	NC	-	not connected
4	O	3.3 V	X_SPI1_CS1 (GPIO1_18 of AM335x)
5	O	3.3 V	X_SPI1_CS0
6	I	3.3 V	X_SPI1_MISO
7	O	3.3 V	X_SPI1_MOSI
8	O	3.3 V	X_SPI1_CLK
9	-	GND	Ground
10	O	3.3 V	VREF_SPI1

Table 58: SPI1 Pin Header X30 Pinout

15.3.12 User programmable GPIOs (X54)

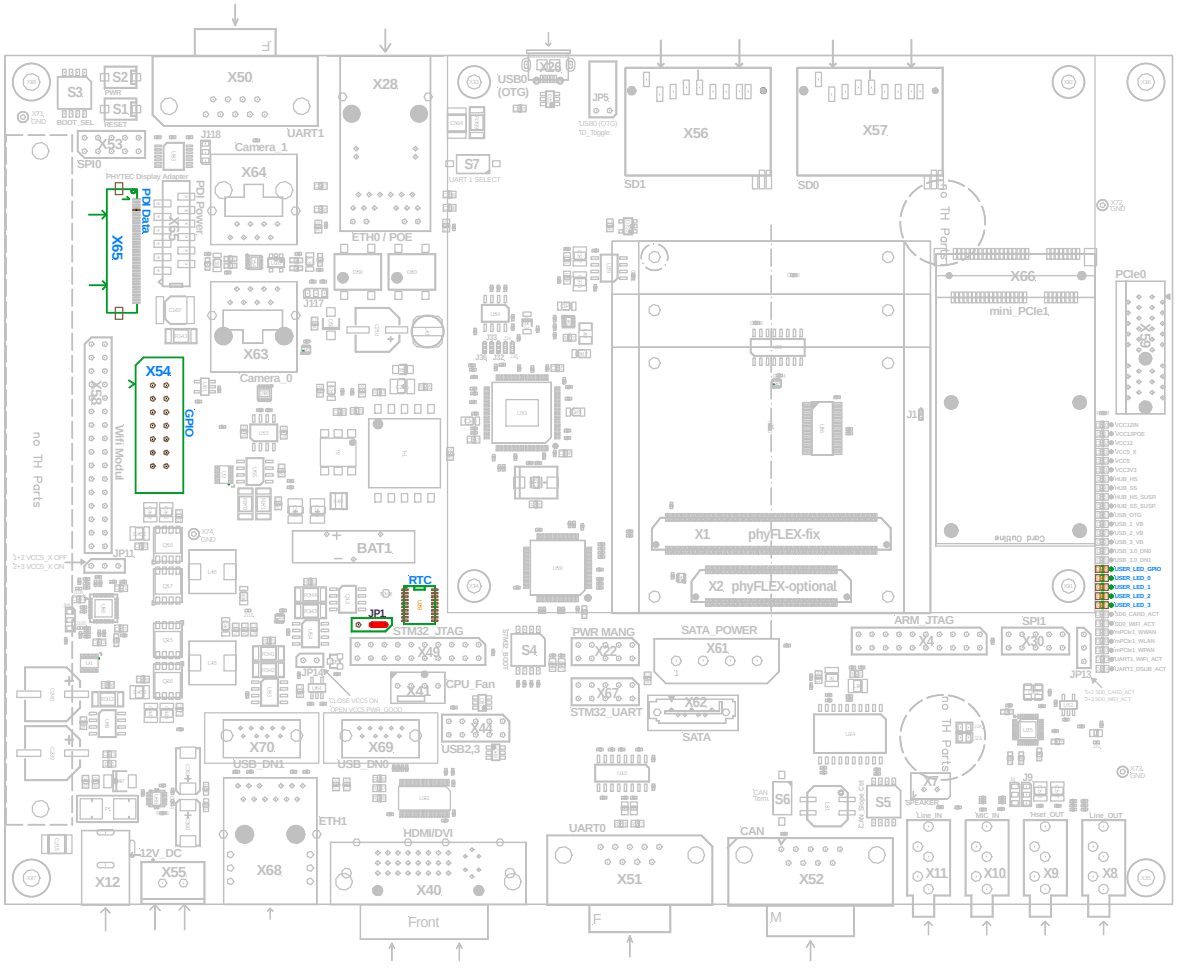


Figure 34: User programmable GPIOs and LEDs

The phyFLEX-AM335x provides 11 GPIOs. GPIO0, GPIO5 and GPIO6 are ports of the AM335x, while GPIO1..4 and GPIO7..10 are realized using a GPIO Expander at U2 (refer to *section 9* for more information). Some GPIOs are reserved for special functions on phyFLEX Carrier Board. All GPIOs are also mapped at GPIO Connector X54. See *Table 59* which function each GPIO has.

GPIO	Function
GPIO0	Interrupt Touch Controller at U6
GPIO5	If JP1 is connected between pin 2 and 3, signal RTC_INT is connected to X_GPIO5
GPIO6	SPI_IRQ at PDI data connector X65 (pin B5)
GPIO10	Connected to User LED D105

Table 59: GPIOs used on the phyFLEX Carrier Board

Pin	ST	SL	Description
1	-	3.3 V	VREF_GPIO
2	I/O	3.3 V	X_GPIO0
3	I/O	3.3 V	X_GPIO1
4	I/O	3.3 V	X_GPIO2
5	I/O	3.3 V	X_GPIO3
6	I/O	3.3 V	X_GPIO4
7	I/O	3.3 V	X_GPIO5
8	I/O	3.3 V	X_GPIO6
9	I/O	3.3 V	X_GPIO7
10	I/O	3.3 V	X_GPIO8
11	I/O	3.3 V	X_GPIO9
12	I/O	3.3 V	X_GPIO10
13	-	GND	Ground
14	-	GND	Ground

Table 60: GPIO Pin Header X54 Pinout

15.3.13 User programmable LEDs

The phyFLEX Carrier Board provides 5 user programmable LEDs.

LED D105, is directly connected to GPIO10 of the phyFLEX-AM335x (pin X1A67). A logic 1 at X_GPIO10 turns the LED on (refer to *section 9*).

The other user programmable LEDs (D86, D97-D99) are controlled by a 4-bit LED dimmer at U52 (at the backside of the CB) which is connected to I2C0 at address 0x62.

The following table lists all user programmable LEDs.

LED	Color	Description
D105	green	User LED connected to GPIO10 (P7 from GPIO Expander U2 on the phyFLEX-Am335x)
D97	red	User LED0 (port LED0 from 4-bit LED dimmer at U52)
D98	yellow	User LED1 (port LED1 from 4-bit LED dimmer at U52)
D99	yellow	User LED2 (port LED2 from 4-bit LED dimmer at U52)
D86	green	User LED3(port LED3 from 4-bit LED dimmer at U52)

Table 61: User Programmable LEDs on the Carrier Board

15.3.14 Secure Digital Memory Card/ MultiMedia Card (X57, X56)

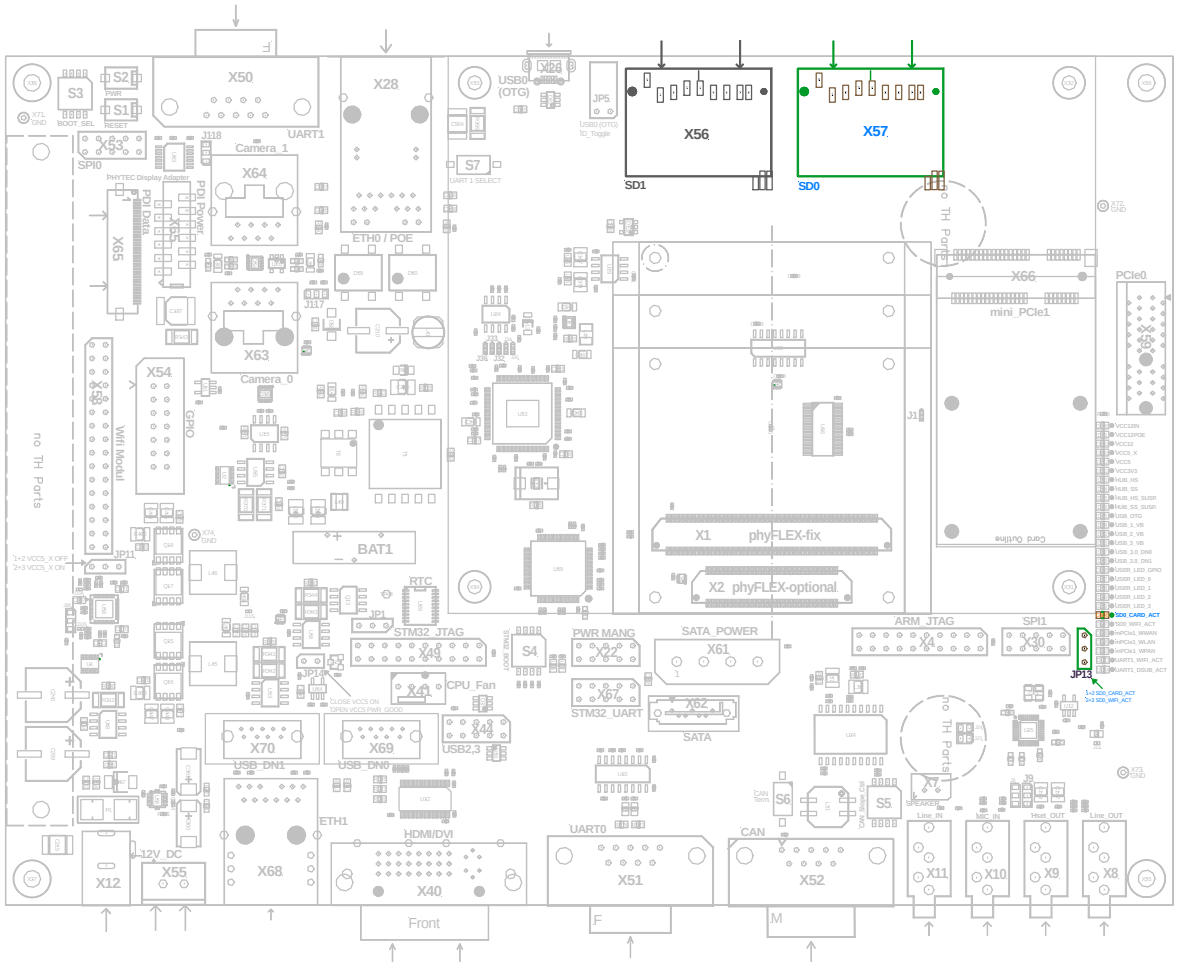


Figure 35: SD / MM Card interfaces at connector X57 and X56

The phyFLEX Carrier Board provides two standard SDHC card slots at X57 and X56 for connection to SD/MM cards. It allows easy and convenient connection to peripheral devices like SD- and MM cards. Power to the SD interface is supplied by inserting the appropriate card into the SD/MMC slot.

The phyFLEX-AM335x provides only one SD/MM card interface (SD0) which connects to X57. SD0 at X57 shares the SDIO signals with the Wi-Fi/Bluetooth connector X58. To use the SD0 card slot at X57, JP13 must be closed at 1 and 2. LED D106 (yellow) shows that card slot SD0 (X57) is active.

Note:
X56 is not supported by the phyFLEX-AM335x SOM.

15.3.15 CPU Fan Connector (X41)

If a CPU Fan is used, the carrier board supports the direct connection of a standard CPU fan with speed control at X41 (see *Figure 16*).

Pin #	Signal Name	Description
1	GND	Ground
2	VCC12	12 V power supply
3	X_PM_TACHO	Fan Speed Signal
4	X_PM_PWM	Speed Control Signal

Table 62: CPU Fan Connector X41

Note:
The signals for CPU fan control are generated from the EMIC (U29) on the phyFLEX-AM335x which requires custom specific programming (refer to *section 12*).

15.3.16 Wi-Fi/Bluetooth Connector (X58)

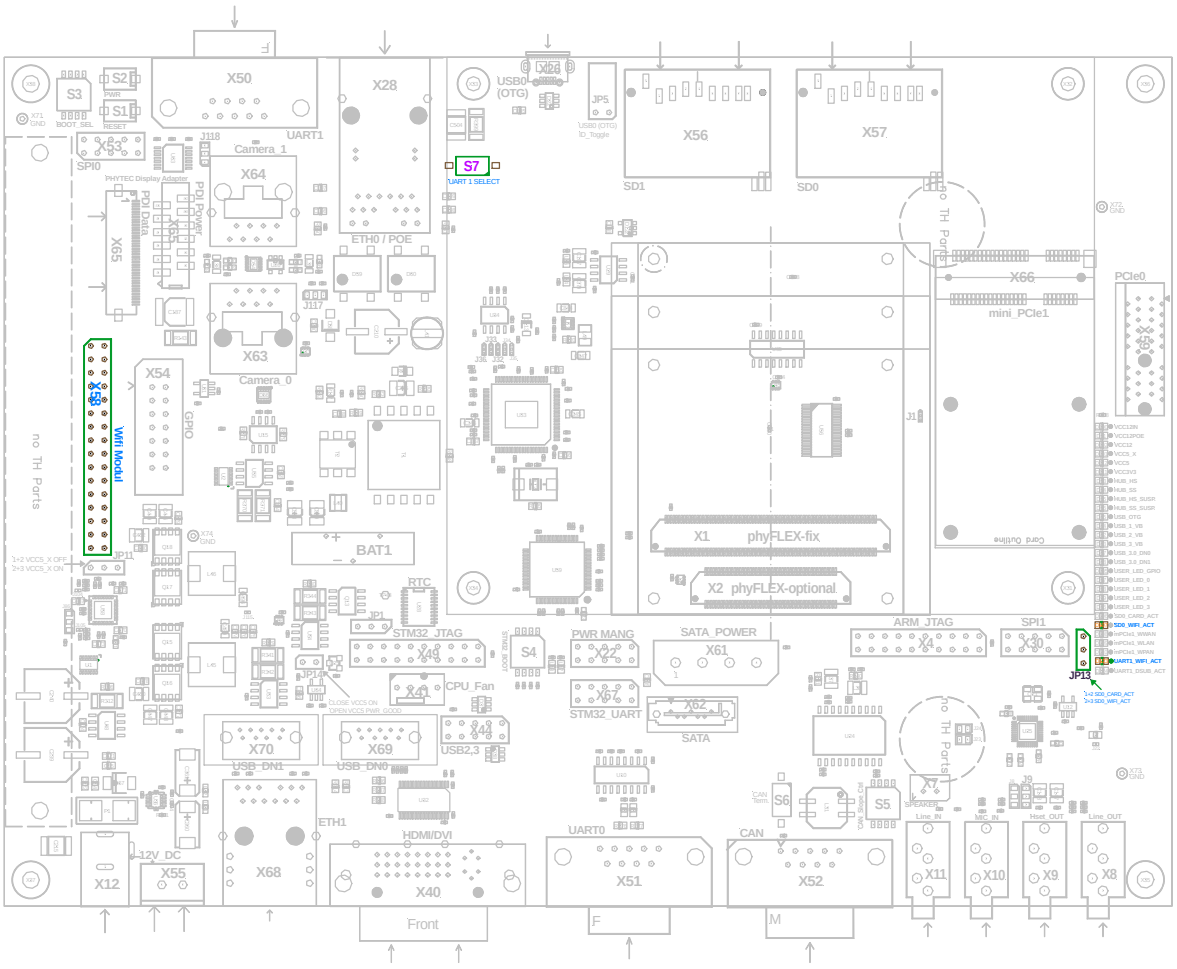


Figure 36: SD / MM Card interfaces at connector X57 and X56

A Wi-Fi/Bluetooth module, such as the PHYTEC PCM-958, can connect to the carrier board's pin header at X58.

Two different interfaces (UART1 and SD0) connect to the Wi-Fi/Bluetooth module.

To provide the TTL signals of UART1 at the Wi-Fi/Bluetooth connector X58 DIP-switch S7 must be open. LED D123 (yellow) indicates that UART1 is available at connector X58.

Use of SDIO for Wi-Fi/Bluetooth requires JP13 to be switched from position 1+2 to 2+3. LED D107 (yellow) indicates that SDIO is available at connector X58. *Table 63* shows the pinout of connector X58.

Pin #	ST	SL	Description
1	-	-	not connected
2	-	GND	Ground
3	-	-	not connected
4	-	1.8 V	VCC1V8
5	-	-	not connected
6	-	1.8 V	VCC1V8
7	-	GND	Ground
8	-	GND	Ground
9	O	3.3 V	UART1_TXD_WIFI (TTL)
10	-	3.3 V	VREF_SD0
11	O	3.3 V	UART1_RTS_WIFI (TTL)
12	-	3.3 V	VREF_SD1
13	I/O	3.3 V	SD0_D5_WLAN
14	-	3.3 V	VCC3V3
15	-	GND	Ground
16	-	3.3 V	VCC3V3
17	I/O	3.3 V	SD0_D4_WLAN
18	-	GND	Ground

Table 63: Wi-Fi/Bluetooth Connector X58

Pin	ST	SL	Description
19	I/O	3.3 V	SD0_D6_WLAN
20	-	-	not connected
21	I/O	3.3 V	SD0_D3_WLAN
22	I	3.3 V	UART1_RXD_WIFI (TTL)
23	-	GND	Ground
24	I	3.3 V	UART1_CTS_WIFI (TTL)
25	I/O	3.3 V	SD0_D2_WLAN
26	-	GND	Ground
27	I/O	3.3 V	SD0_D1_WLAN
28	I/O	3.3 V	SD0_D7_WLAN
29	I/O	3.3 V	SD0_D0_WLAN
30	I/O	3.3 V	SD0_CMD_WLAN
31	-	GND -	Ground
32	O	3.3 V	SD0_CLK_WLAN

Table 63: Wi-Fi/Bluetooth Connector X58 (continued)

15.3.17 Boot Mode Selection (S3)

The boot mode DIP Switch S3 (see *Figure 16*) is provided to configure the boot mode of the phyFLEX-AM335x after reset. This DIP Switch allows choosing different boot sources. The following table gives an overview of the different boot sources. Refer to *sections 4.4* and *5* for more information on the boot configuration.

Note:
The following table describes only settings suitable for the phyFLEX-AM335x. Other settings must not be used with the phyFLEX-AM335x.

Caution!
The boot signals are equipped with pull-up resistors, thus the standard signal level is high (Off position of DIP-switch S3). In order to pull a particular signal low the corresponding switch of DIP-switch S3 must be set to the ON position.

Boot Mode	X_BOOT0 (S3_1)	X_BOOT1 (S3_2)	X_BOOT2 (S3_3)	BOOT Source
0	**1**	**1**	**1**	NAND,(NANDI2C,MMC0,UART0)
1	0	1	1	SPI0, CS0 (on board SPI Flash if populated, same as mode 2), (MMC0,EMAC1,UART0)
2	1	0	1	SPI0, CS0 (on board SPI Flash if populated, same as mode 1), (MMC0,EMAC1,UART0)
3	0	0	1	MMC0, (SPI0, UART0, USB0)
4	1	1	0	UART0, (SPI0, NAND, NANDI2C)
5	0	1	0	No Sata available →Boot Mode 0 is aktiv
6	1	0	0	Serial USB OTG USB0, (NAND, SPI0, MMC0)
7	0	0	0	EMAC1(ETH1), (XIP (MUX1), SPI0, NANDI2C)

Table 64: phyFLEX Carrier Board DIP Switch S3 Descriptions[1]

15.3.18 System Reset Button (S1)

The phyFLEX Carrier Board is equipped with a system reset button at S1 (see *Figure 16*). Pressing the button pulls the reset input X_nPM_RESET_IN low which will reset the phyFLEX mounted on the phyFLEX Carrier Board. In the sequel the phyFLEX module generates the signal X_nPM_RESET_OUT, which resets the peripheral devices on the phyFLEX Carrier Board, such as the USB Hub, etc.

[1]: Default settings are in **bold blue** text

15.3.19 System Power On/Off/Wake Button (S2)

The phyFLEX Carrier Board is equipped with a system Power On/Off/Wake Button (S2; see *Figure 16*). Pressing this button less than 5 seconds will wake up the phyFLEX-AM335x module and the peripherals on the carrier board, or will turn on the system, if it is powered off. Pressing this button more than 5 seconds will turn off the system without proper shut down of the operating system.

15.3.20 JTAG Interface (X4)

The JTAG interface of the phyFLEX-AM335x is accessible at connector X4 on the carrier board (see *Figure 16*). This interface is compliant with JTAG specification IEEE 1149.1 or IEEE 1149.7. No jumper settings are necessary for using the JTAG port. The following table describes the signal configuration at X4. When referencing contact numbers note that pin 1 located at the angled corner. Pins towards the labeling "ARM_JTAG" are odd numbered

Pin #	Signal Name	ST	SL	Description
1	VREF_JTAG	O	3.3 V	JTAG reference voltage (VREF_JTAG via 100 Ohm resistor)
2	VREF_JTAG	O	3.3 V	JTAG reference voltage
3	X_nJTAG0_TRSTB	I	3.3 V	JTAG Test Reset
4, 6, 8, 10, 12, 14, 18, 20	GND	-		Ground
5	X_nJTAG0_TDI	I	3.3 V	JTAG Test Data Input
7	X_JTAG0_TMS	I/O	3.3 V	JTAG Test Mode Select Signal
9	X_JTAG0_TCK	I	3.3 V	JTAG Test Clock Signal
11	X_JTAG0_RTCLK	O	3.3 V	JTAG Return Test Clock Signal
13	X_JTAG0_TDO	O	3.3 V	JTAG Test Data Output
15	X_nPM_RESET_IN	I	3.3 V	System Reset
17	not connected	-	-	-
19	not connected	-	-	-

Table 65: JTAG Connector X4

15.3.21 RTC at U28

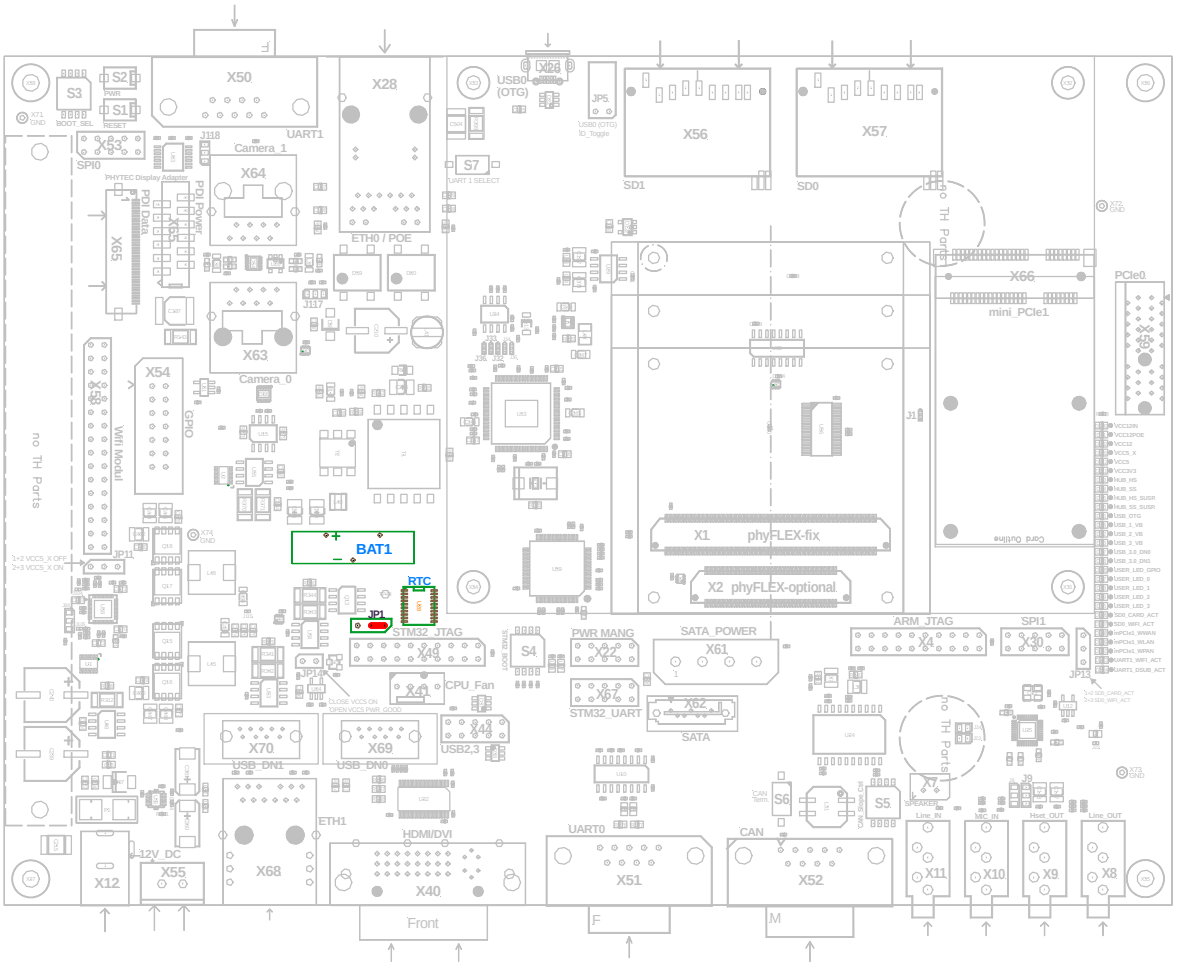


Figure 37: RTC with Battery Buffer

For real-time or time-driven applications, the phyFLEX Carrier Board is equipped with an RTC-8564 Real-Time Clock at U28. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0x51 (7 MSB)
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: = 275 nA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I^2C bus (address 0x51). Since the phyFLEX-AM335x is equipped with an internal I^2C controller, the I^2C protocol is processed very effectively without extensive processor action (refer also to *section 8.5*)

The Real-Time Clock also provides an interrupt output that extends to jumper JP1. Jumper JP1 allows to connect the RTC interrupt to the X_nPM_ ON/WAKEUP/OFF input or to X_GPIO5 of the phyFLEX-AM335x (GPIO1_23 of the AM335x). An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

Position	Description
1+2	**RTC Interrupt connected to X_nPM_ ON/WAKEUP/OFF**
2+3	RTC Interrupt connected to X_GPIO5 (GPIO1_23 of the AM335x)

Table 66: RTC Interrupt Configuration JP1

Note:
After connecting the supply voltage the Real-Time Clock generates no interrupt. The RTC must be first initialized (see *RTC Data Sheet* for more information).

Use of a coin cell at BAT1 allows to buffer the RTC.

15.3.22 Environment Management IC (EMIC) (U59)

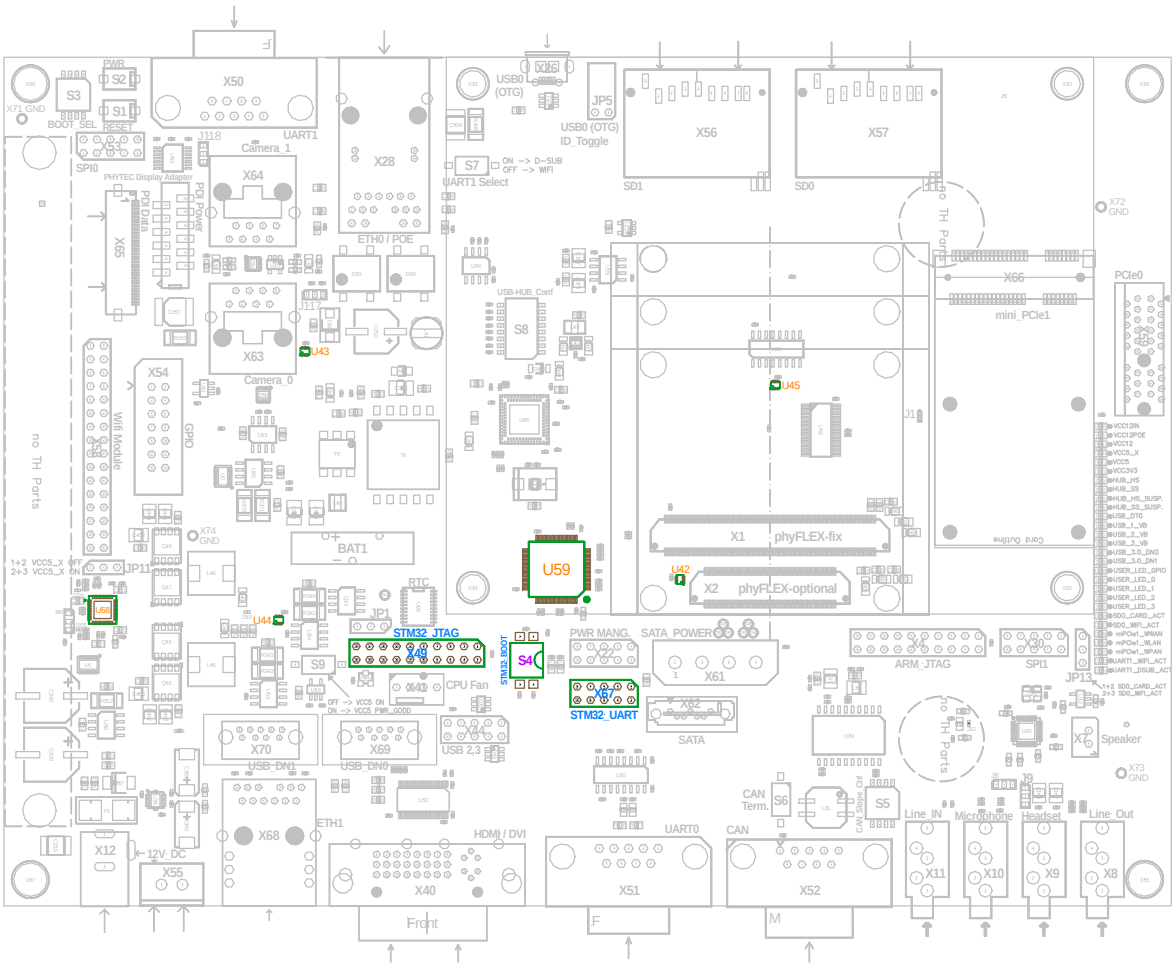


Figure 38: EMIC and supporting Components (top view)

The optional Environment Management IC (EMIC) at U59 on the carrier board gives the possibility to detect, monitor and record particular physical parameter such as current consumption, temperature und voltages. Furthermore the Environment Management IC comes with an additional serial interface and an I^2C Management bus.

The Environment Management IC can be programmed via JTAG connector X49 (refer to *Table 69*).

Note:
There is no software available for the EMIC. If you need further information, or a quotation for a custom software development, please contact PHYTEC at sales@phytec.de.

Data such as current consumption, voltage and state of control signals is collected via digital IOs of the EMIC, while the temperatures measured by sensors U42 – U45 is read via I^2C interface.

Table 67 shows the physical parameters which can be measured by the EMIC at U59 and the corresponding ports, whereas *Table 68* sums up the data collected via I^2C interface.

Port	Signal	Description
		Suplly Voltages
PA0	VCC12_IN_SENSE	12 Volt supply voltage at connector X12, or X55
PA1	VCC12_POE_SENSE	12 Volt supply voltage at connector X12, or X55
PA2	VCC12_SENSE	12 Volt supply voltage at connector X12, or X55
PA3	VCC5_SENSE	12 Volt supply voltage at connector X12, or X55
PA4	VCC3V3_SENSE	
		Suplly Currents
PC0	Current_VCC12_IN	Entire supply current through X12, or X55
PC1	Current_VCC12_POE	Entire supply current throughPOE at X28
PC2	Current_VCC5	Supply current of all 5 V components on the carrier board except the phyFLEX module
PC3	Current_VCC3V3	Supply current of all 3.3 V components on the carrier board
		Control Signals
PC12	PGOOD_VCC5	Power good signal related to the 5 V supply voltage[1]
PC13	PGOOD_VCC3V3	Power good signal related to the 3.3 V supply voltage[1]
		Temperature Allerts
PC6	ALERT1	Overtemperature alert of module connectors temperature (U42)
PC7	ALERT2	Overtemperature alert of POE circuitry temperature (U43)
PC8	ALERT3	Overtemperature alert of power circuitry temperature (U44)
PC9	ALERT4	Overtemperature alert of module temperature (U45)

Table 67: Environment Management IC (EMIC) Measured Variables

The table below lists the I^2C addresses of the four temperature sensors, while *Figure 38* shows the location of the sensors.

Device #	I^2C Address	Position of the Temperature Sensor	Alert # (s. *Table 67)*
		Temperature	
U42	0x49	Module connector	ALERT1
U43	0x48	POE circuitry	ALERT2
U44	0x4B	Power circuitry	ALERT3
U45	0x4A	Underneath the SOM	ALERT4

Table 68: Environment Management IC (EMIC) Measured Data via I^2C Interface

[1]: The 2 Power Good inputs connect to the Power Good Outputs of the 5 V/ 3.3 V regulator at U58

Note:
To avoid any conflicts when connecting external I^2C devices to the EMIC's I^2C bus the addresses of the on-board temperature sensors must be considered.

Pin #	Signal Name	ST	SL	Description
1	VREF_JTAG	O	3.3 V	JTAG reference voltage (VCC3V3 via 100 Ohm resistor)
2	VREF_JTAG	O	3.3 V	JTAG reference voltage (VCC3V3)
3	nJTAG_STM32_TRST	I	3.3 V	JTAG Test Reset
4, 6, 8, 10, 12, 14, 18, 20	GND	-		Ground
5	JTAG_STM32_TDI	I	3.3 V	JTAG Test Data Input
7	JTAG_STM32_TMS	I/O	3.3 V	JTAG Test Mode Select Signal
9	JTAG_STM32_TCK	I	3.3 V	JTAG Test Clock Signal
11	not connected	-	-	-
13	JTAG_STM32_TDO	O	3.3 V	JTAG Test Data Output
15	JTAG_STM32_RST	I	3.3 V	Reset
17	not connected	-	-	-
19	not connected	-	-	-

Table 69: EMIC JTAG Connector X49

The EMIC at U59 provides an additional UART interface which is available at pin header connector X67. The following table shows the pin-out of connector X67.

Pin #	Signal Name	ST	SL	Description
1, 2, 4, 6, 7, 8, 10	not connected	-	-	-
3	EMIC_UART_TX	O	3.3 V	EMIC UART serial transmit signal
5	EMIC_UART_RX	I	3.3 V	EMIC UART serialdata receive signal
9	GND	-	-	Ground 0 V

Table 70: Environment Management IC (EMIC) UART Interface Connector X67

The EMIC has different internal memory devices. The following table shows the different Boot Sources depending on the configuration of DIP-switch S4.

Boot Mode	PB2/BOOT1	BOOT0	DIP-switch S4		Bootsource
			2	1	
0	X	0	X	Off	User Flash memory
1 (optional)	0	1	Off	On	System memory
2 (optional)	1	1	On	On	Embedded SRAM

Table 71: EMIC Boot Mode Selection S4

16 Revision History

Date	Version numbers	Changes in this manual
28.01.2014	Manual L-798e_1	First edition. Describes the phyFLEX-AM335x (PCB. No. 1386.3) with phyFLEX Carrier Board (PCB. No. 1364.5).
20.08.2014	Manual L-798e_2	Second edition. Describes the phyFLEX-AM335x (PCB. No. 1386.3) with phyFLEX Carrier Board (PCB. No. 1364.6).

Index

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Document number: **L-798e_2, August 2014**

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