PHYTEC

phyCORE-TC1796

Hardware Manual

Edition Sept. 2010

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Preface

This phyCORE-TC1796 Hardware Manual describes the board's design and functions. Precise specifications for Infineon’s TC1796 TriCore microcontroller series controller can be found in the enclosed microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration of Electro Magnetic Conformance of the PHYTEC phyCORE-TC1796

PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Caution:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformance only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header row connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-TC1796 is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports all common 8- and 16-bit as well as selected 32-bit controllers in two ways:

(1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform

(2) as insert-ready, fully functional micro-, mini- and phyCORE OEM modules, which can be embedded directly into the user's peripheral hardware, design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-TC1796 belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a subminiature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD components and laser-drilled Microvias are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-TC1796 is a subminiature (71,5 x 57) insert-ready Single Board Computer populated with Infineon's TC1796 Tricore microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density pitch (0.635 mm) connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the Infineon TC1796 Tricore microcontroller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-TC1796.

The phyCORE-TC1796 offers the following features:

- subminiature SBC in phyCORE dimensions 71,5 x 57 mm with two 160-pin high-density (0.635 mm) Molex connectors, enabling it to be plugged like a “big chip” into target application
- Processor: Infineon Tricore TC1796, 20 MHz external clock
- **Internal Components of the phyCORE-TC1796:**
  - High performance 32-bit TriCORE CPU
  - 2MByte Program Flash Memory
  - DMA Controller
  - two synchronous serial interfaces
  - two UARTs
  - MultiCAN 2.0B (4 Nodes) (one CAN node supports TTCAN)
  - Capture and Compare units
  - Two General Purpose Timer Unit (GPTU) timers with additional Local Timer Cell Array (LTCA2)
  - Two 16-channel Analog-to-Digital Converter units (ADC) with selectable 8-bit, 10-bit, or 12-bit resolution
  - One 4-channel Fast Analog-to-Digital Converter unit (FADC)
  - 44 analog input lines for ADC and FADC
  - Multi-purpose I/O signals
- **Memory Configuration**[1]**:**
  - SRAM (2 Banks): 8MByte maximum
  - Flash-ROM: 64 MByte Intel Strata Flash maximum;
  - SPI memory: 32Kbyte EEPROM or 2MByte Flash
- two I^2C – Bus Master –Controller (SC18IS600)
- I^2C Real-Time Clock with calendar and alarm functions
- Ethernet-Controller with HW TCP/IP-Stack (W5300) 10/100Mbit (PHY)
- Optional USB to UART Bridge
- UART: RS-232 transceiver for two channels (RxD/TxD); TTL level can be configured
- MultiCAN port: SN65HVD23x transceiver for all channels; TTL level can be configured
- JTAG/Debug port

[1]: Please contact PHYTEC for more information about additional modul configurations.

Operating temperature:: -40°C to +85°C

1.1 Block Diagram

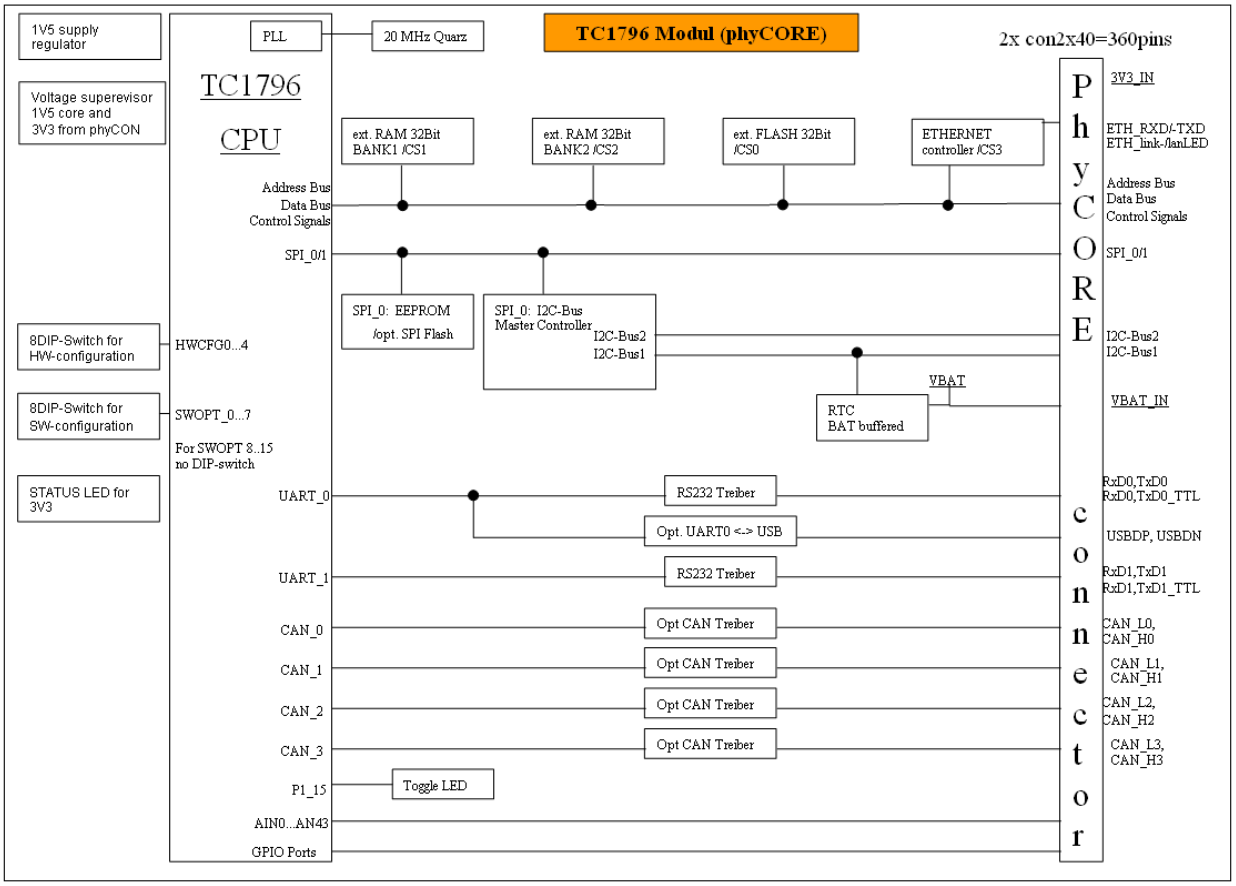

Figure 1: Block Diagram phyCORE-TC1796

1.2 View of the phyCORE-TC1796

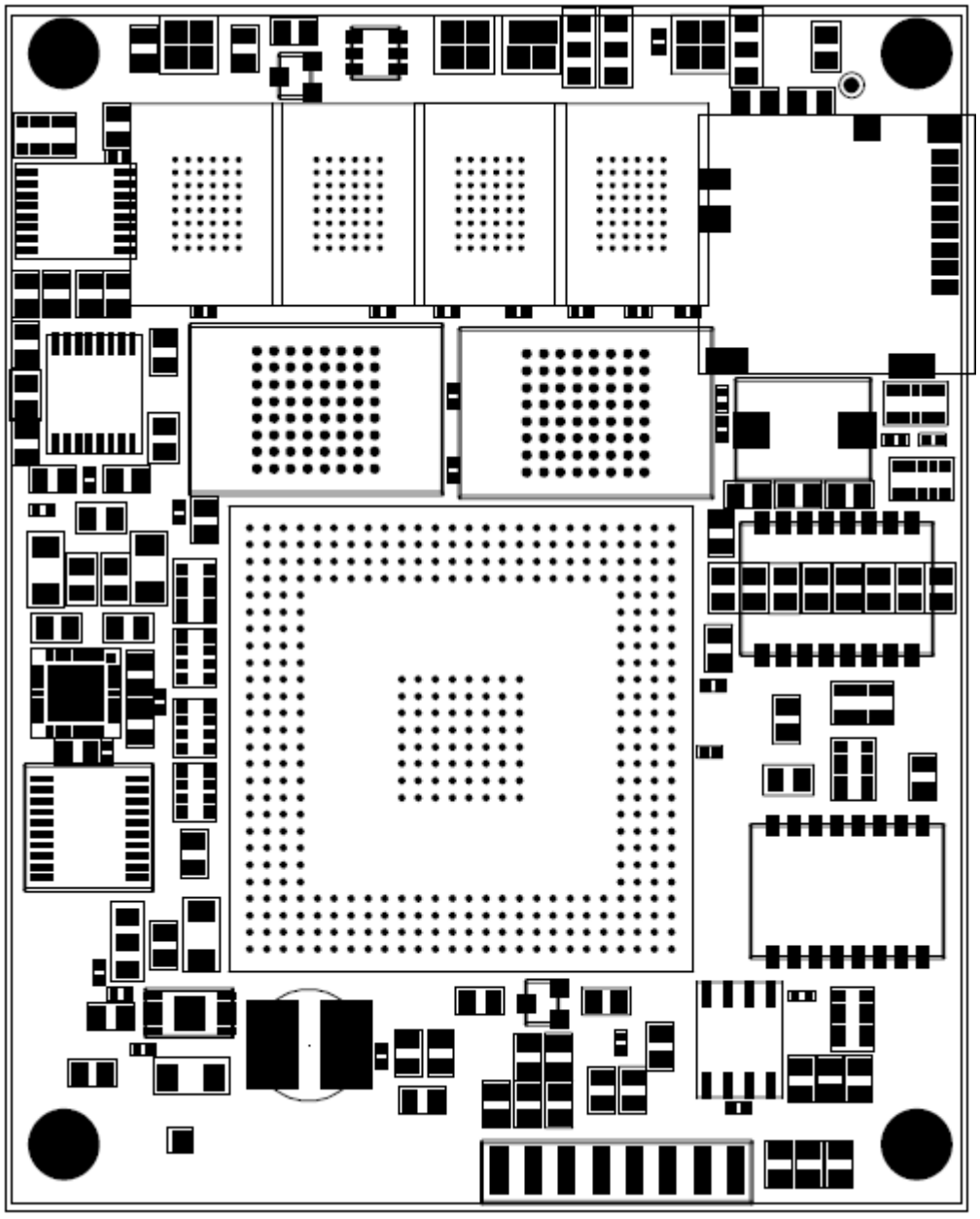

Figure 2: View of the phyCORE-TC1796 (Controller Side)

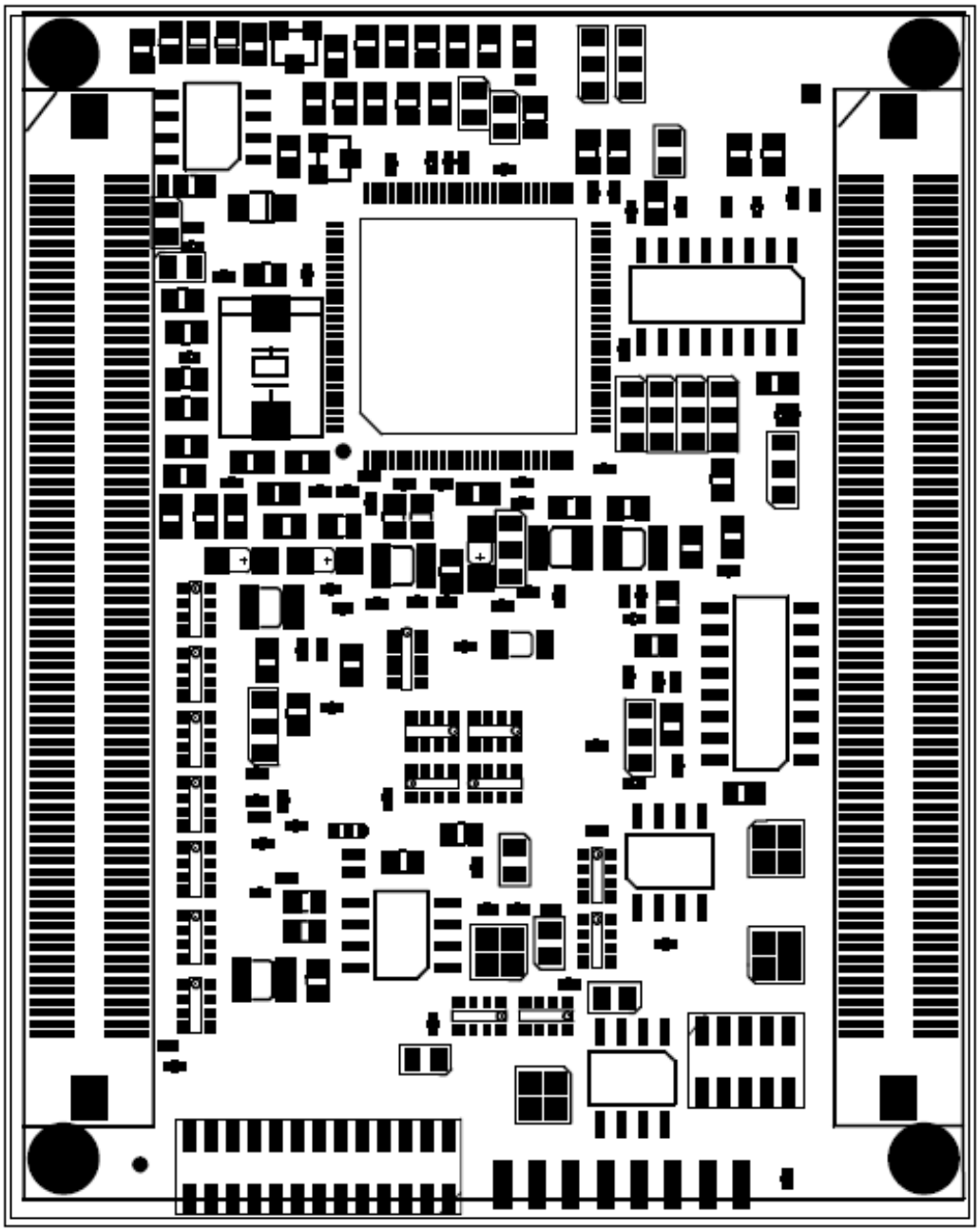

Figure 3: View of the phyCORE-TC1796 (Connector Side)

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector). This allows the phyCORE-TC1796 to be plugged into any target application like a "big chip".

A new numbering scheme for the pins on the phyCORE-connector has been introduced with the phyCORE specifications. This enables quick and easy identification of desired pins and minimizes errors when matching pins on the phyCORE module with the phyCORE-connector on the appropriate PHYTEC Development Board or in user target circuitry.

The numbering scheme for the phyCORE-connector is based on a two dimensional matrix in which column positions are identified by a letter and row position by a number. Pin 1A, for example, is always located in the upper left hand corner of the matrix. The pin numbering values increase moving down on the board. Lettering of the pin connector rows progresses alphabetically from left to right (*refer to Figure 4*).

The numbered matrix can be aligned with the phyCORE-TC1796 (viewed from above; phyCORE-connector pointing down) or with the socket of the corresponding phyCORE Development Board/user target circuitry. The upper left-hand corner of the numbered matrix (pin 1A) is thus covered with the corner of the phyCORE-TC1796 marked with a white triangle. The numbering scheme is always in relation to the PCB as viewed from above, even if all connector contacts extend to the bottom of the module.

The numbering scheme is thus consistent for both the module's phyCORE-connector as well as mating connectors on the phyCORE Development Board or target hardware, thereby considerably reducing the risk of pin identification errors.

Since the pins are exactly defined according to the numbered matrix previously described, the phyCORE-connector is usually assigned a single designator for its position (X3 for example). In this manner the phyCORE-connector comprises a single, logical unit regardless of the fact that it could consist of more than one physical socketed connector.

The following figure (*Figure 4*) illustrates the numbered matrix system. It shows a phyCORE-TC1796 with SMT phyCORE-connectors on its underside.

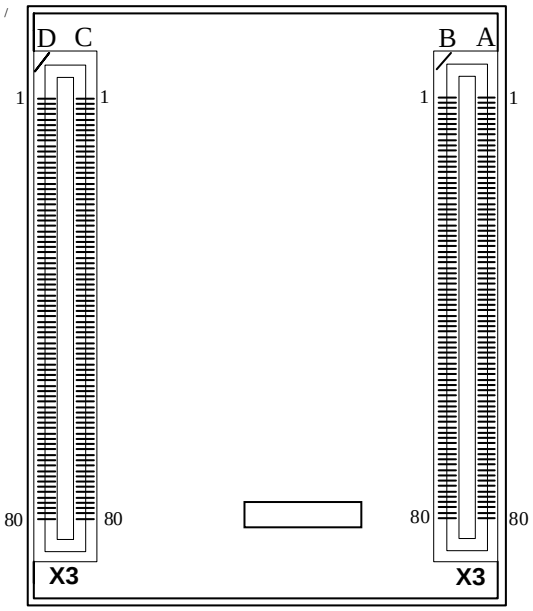

Figure 4: Pinout of the phyCORE-Connector (view from Connector Side)

Many of the controller port pins accessible at the connectors along the edges of the board have been assigned alternate functions that can be activated via software.

Table 1 provides an overview of the pinout of the phyCORE-connector (X3) , as well as descriptions of possible alternative functions. *Please refer to the Infineon TC1796 User's Manual/Data Sheet for details on the functions and features of controller signals and port pins*.

Pin Number	Signal	I/O	Description
Pin Row X3A			
1A	NC	-	not connected
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A	GND	-	Ground 0 V
3A	P11	I/O	Microcontroller's port P1.1, used as interrupt input (REQ1)for onboard I2C Master controller U11 P1.1 free to use if J39 is NOT populated **default: J39 is populated**
4A	/NMI	I	/NMI Interrupt of the controller
5A	/CS3	O	Microcontroller's Chip Select output. Used for onboard Ethernet Controller U21 Free to use if the (U21) is NOT populated or jumper J24 is open *(refer to jumper J24)*
6A	/ADV	O	Microcontroller's Address Valid Output
8A	/BC0	O	Microcontroller´s Byte Control signal for data lines D[0..7].
9A, 10A, 11A, 13A, 14A, 15A, 16A, 18A, 24A, 25A, 26A, 28A	A1, A2, A4, A7, A9, A10, A12, A15, A17, A18, A20, A23	O	Microcontroller's Address lines, are used to access on-board memory
19A, 20A, 21A, 23A, 29A, 30A, 31A, 33A, 38A, 39A, 40A, 41A, 43A, 44A, 45A, 46A	D1, D2, D4, D7, D9, D10, D12, D15, D17, D19, D20, D22, D25, D27, D28, D30	I/O	Microcontroller´s Data lines, are used to access on-board memory
34A	/WAIT	I	Microcontroller's wait signal
35A	/CS0	O	Microcontroller's Chip Select output. Used for onboard ext.Flash U3/U4 Free to use if (U3/U4) is NOT populated or jumper J11 is open *(refer to jumper J11)*
36A	/HLDA	O	Hold acknowledge I/O of the Microcontroller

Pin Number	Signal	I/O	Description
Pin Row X3A			
48A	LAN_/CS	I	Chip Select input of the onboard Ethernet Controller (U21). Can be used if jumper J24 is open *(refer to jumper J24)*
49A	/WR	O	Microcontroller's write signal
50A	BFCLKI	I	Microcontroller´s burst flash clock input (clock feedback)
51A	BFCLKO	O	Microcontroller´s Burst flash clock output
53A	/CSRAM2	I	Chip Select input of the second RAM BANK. can be used if jumper J18 is open *(refer to jumper J18)*
54A	P115	I/O	Microcontroller's port P1.15 Used for onboard red LED *(refer to jumper J19)*
55A	P113	I/O	Microcontroller´s port P1.13
56A	P111	I/O	Microcontroller´s port P1.11
58A	P18	I/O	Microcontroller´s port P1.8
59A	P17	I/O	Microcontroller´s port P1.7
60A	P16	I/O	Microcontroller´s port P1.6
61A	P14	I/O	Microcontroller´s port P1.4
63A	P314	I/O	Microcontroller´s port P3.14
64A	P312	I/O	Microcontroller´s port P3.12
65A	P311	I/O	Microcontroller´s port P3.11
66A	P39	I/O	Microcontroller´s port P3.9
68A	P36	I/O	Microcontroller´s port P3.6
69A	P34	I/O	Microcontroller´s port P3.4
70A	P33	I/O	Microcontroller´s port P3.3
71A	P31	I/O	Microcontroller´s port P3.1
73A	P214	I/O	Microcontroller´s port P2.14
74A	P212	I/O	Microcontroller´s port P2.12
75A	P211	I/O	Microcontroller´s port P2.11
76A	P29	I/O	Microcontroller´s port P2.9
78A	P26	I/O	Microcontroller´s port P2.6
79A	P24	I/O	Microcontroller´s port P2.4
80A	P23	I/O	Microcontroller´s port P2.3

Pin Number	Signal	I/O	Description
Pin Row X3B			
1B	RTC_CLKOUT	O	Realtime Clock Clockout (*refer to jumper J35*)
2B	P10	I/O	Microcontroller´s port P1.0, used as interrupt (REQ0) input for onboard Ethernet controller U21 P1.1 free to use if J25 is open *(refer to jumper J25)*
3B	P12	I/O	Microcontroller´s port P1.2 used as interrupt (REQ2) input for onboard I2C Master controller U12 P1.2 free to use if J40 is NOT populated **default: J40 is populated**
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B	GND		Ground 0 V
5B	/CS2	O	Microcontroller´s Chip Select signal. Used for second onboard SRAM-BANK U19/U20 Free to use if the second RAM-Bank is NOT populated or Jumper J18 is open *(refer to jumper J18)*
6B	/CS1	I/O	Microcontroller´s Chip Select signal. Used for first onboard SRAM-BANK U17/U18 Free to use if the first RAM-Bank is NOT populated or Jumper J17 is open *(refer to jumper J17)*
7B	x/RD	O	Microcontroller´s read signal
8B, 10B, 11B, 12B, 13B, 15B, 16B, 17B, 23B, 25B, 26B, 27B	A0, A3, A5, A6, A8, A11, A13, A14, A16, A19, A21, A22	O	Microcontroller´s Address lines, are used to access on-board memory
18B, 20B, 21B, 22B, 28B, 30B, 31B, 32B, 37B, 38B, 40B, 41B, 42B, 43B, 45B, 46B	D0, D3, D5, D6, D8,D11, D13, D14, D16, D18, D21, D23, D24, D26, D29, D31	I/O	Microcontroller´s Data lines, are used to access on-board memory
33B	/BC1	O	Microcontroller´s Byte control signal for data lines D[8..15].
35B	/HOLD	I	Microcontroller´s hold request input
36B	/BREQ	O	Microcontroller´s EBU Bus request
47B	/CSCOMB	O	Microcontroller´s Chip Select Output for combination function
48B	MR/W	O	Microcontroller´s Motorola-style Read/Write output
50B	/ADV	O	Microcontroller´s address valid output

Pin Number	Signal	I/O	Description
Pin Row X3B			
51B	/BAA	O	Microcontroller´s Burst address advance output
52B	/BC2	O	Microcontroller´s Byte control signal for data lines D[16..23].
53B	/BC3	O	Microcontroller´s Byte control signal for data lines D[24..31].
55B	P114	I/O	Microcontroller´s port P1.14 used as microSD card detect. refer to section 14
56B	P112	I/O	Microcontroller´s port P1.12
57B	P110	I/O	Microcontroller´s port P1.10
58B	P19	I/O	Microcontroller´s port P1.9
60B	P15	I/O	Microcontroller´s port P1.5
61B	P13	I/O	Microcontroller´s port P1.3
62B	P315	I/O	Microcontroller´s port P3.15
63B	P313	I/O	Microcontroller´s port P3.13
65B	P310	I/O	Microcontroller´s port P3.10
66B	P38	I/O	Microcontroller´s port P3.8
67B	P37	I/O	Microcontroller´s port P3.7
68B	P35	I/O	Microcontroller´s port P3.5
70B	P32	I/O	Microcontroller´s port P3.2
71B	P30	I/O	Microcontroller´s port P3.0
72B	P215	I/O	Microcontroller´s port P2.15
73B	P213	I/O	Microcontroller´s port P2.13
75B	P210	I/O	Microcontroller´s port P2.10
76B	P28	I/O	Microcontroller´s port P2.8
77B	P27	I/O	Microcontroller´s port P2.7
78B	P25	I/O	Microcontroller´s port P2.5
80B	P22	I/O	Microcontroller´s port P2.2 used as SLSO2 (SSC Slave Select Output2) for onboard I2C Master controller U12 *refer to jumper 15*

Pin Number	Signal	I/O	Description
Pin Row X3C			
1C, 2C	3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C,	GND	-	Ground 0 V
4C, 5C	NC P9.4 P5.7	-	not connected pins until revision PL2197.1 since revision PL2197.2 X3C-4 is P9.4 X3C-5 is P5.7
6C	VBAT_IN	I	Supply voltage for the RTC and Low Power SRAM data retention *(refer to J36, J37)*
8C	RESOUT	O	High active Reset-output, generated by inverting the /Reset output of the voltage supervisor U16 with FET Q4 **Caution: do not short the RESOUT Signal.** **It cause damage to the MOSFET Q4**
9C	/BOOT	I	Following a power-on reset (/PORST) the Boot configuration of the processor is read over the inputs HWCFG[3..0]. The state of these inputs is determined via the /BOOT signal . /BOOT = low => Boot config. via S1 (1-4) /BOOT = high => Boot config. via S1 (5-8) (please refer to chapter 5 "Power-On-Reset Characteristics ") Boot config. via J3-J10 are NOT accessible If S1 is populated (default) because the pads of these jumpers are below DIP-switchS1 *(refer to jumper J3-J10)* Use Dip-switch S2 to configure SWOPT0-7
10C	/HDRST	I/O	Microcontroller´s hard-reset signal, /HDRST is controlled by open-drain drivers
11C	/PORST	I	Microcontroller´s power-on reset, the boot configuration is fetched following a power-on reset
13C, 14C, 15C 16C	 P82 P84 P85 P87	I/O	I/O port P8 Alternative: signals of MSC1 Interface if RN24 is populated **default: RN24 is NOT populated** Microcontroller´s port P8.2 Microcontroller´s port P8.4 Microcontroller´s port P8.5 Microcontroller´s port P8.7
18C	CAN_H1	I/O	CANH output of the CAN transceiver for the 2nd CAN node Alternative: port 6.11 *(refer to jumper J42)*
19C	RXD1_TTL	I	Receive line (A) of the 2nd TC1796 UART Alternative: port P5.2. If the alternative function is used, solder jumper J34 must be open in order to disconnect the RS-232 transceiver from the signal

Pin Number	Signal	I/O	Description
Pin Row X3C			
20C	TXD1_TTL	O	Transmit line (A) of the 2nd TC1796 UART Alternative: port P5.3
21C	RxD1__RS232	I	RxD input of the RS-232 transceiver for the 2nd serial interface, J34 must be closed to use this interface *(refer to jumper J34)*
23C	TxD1_RS232	O	TxD output of the RS-232 transceiver for the 2nd serial interface, J32 must be closed to use this interface *(refer to jumper J32)*
24C	SDA1	I/O	IIC Data Line 1 of I2C Master controller U12
25C	SCL1	O	IIC clock line 1 of I2C Master controller U12
26C	MRST1	I/O	Master transmit / slave receive output / input of the 2nd TC1796 synchronous serial interface Alternative : port P6.5
28C	MTSR1	I/O	Master receive / slave transmit input / output of the 2nd TC1796 synchronous serial interface Alternative : port P6.4
29C	SCLK1	I/O	SSC1 clock input/output of the 2nd TC1796 synchronous serial interface Alternative : port P.6.6
30C	5V_VBUS	I	USB-VBUS (5V) input for opt. bus-powered USB to ASC0 Bridge (U10)
31C	SCL0	I/O	IIC of I2C Master controller U11
33C	E_LINK	O	Link Good signal from the on-board Ethernet Controller U21 *Altern* .***refer to Appendice A***
34C	E_SPEED	O	Speed indication from the on-board Ethernet Controller U21 *Altern.* ***refer to Appendice A***
35C	E_RX-	I	RxD- input line of the on-board Ethernet Controller U21 *Altern.* ***refer to Appendice A***
36C	E_TX-	O	TxD- output line of the on-board Ethernet Controller U21 *Altern.* ***refer to Appendice A***
38C	TRCLK	O	Trace Clock for OCDS Level 2 Debug Trace Lines
39C	/BRKIN	I	Microcontroller´s OCDS Break Input (please refer to chapter 5 “Power-On-Reset Characteristics“)
40C	/BRKOUT	I/O	Microcontroller´s OCDS Break Out
41C	/TRST	I	Microcontroller´s JTAG Reset Input
43C	CAN_L2	I/O	CANL output of the CAN transceiver for the 3rd TC1796 CAN node Alternative: port 6.12 *(refer to jumper J43)*
44C	CAN_H2	I/O	CANH output of the CAN transceiver for the 3rd TC1796 CAN node Alternative: port 6.13 *(refer to jumper J43)*

Pin Number	Signal	I/O	Description
Pin Row X3C			
45C	CAN_L3	I/O	CANL output of the CAN transceiver for the 4th TC1796 CAN node Alternative: port 6.14 *(refer to jumper J44)*
46C,	P55	I/O	Microcontroller´s port P5.5
			Microcontroller´s I/O Port 7
48C,	P71	I/O	Alternative : AD0EMUX2
49C,	P73	I/O	Alternative : AD0EMUX1
50C	P74	I/O	
51C	P76	I/O	Alternative : AD1EMUX0
		I	Analog Inputs of TC1796 **AN0-AN43 are onboard connected to I/O- ports through RN9-RN18, R29, R30 per default** in order to expose more TC1796 I/O-ports to the phyCORE- connector X3.
53C,	AN41		
54C,	AN40		Alternative: Microcontroller´s P5.7
55C,	AN38		Alternative: Microcontroller´s P9.8
56C,	AN36		Alternative: Microcontroller´s P9.6
58C,	AN33		Alternative: Microcontroller´s P9.4
59C,	AN32		Alternative: Microcontroller´s P9.1
60C	AN31		Alternative: Microcontroller´s P9.0
61C	AN30		Alternative: Microcontroller´s P4.15
63C	AN27		Alternative: Microcontroller´s P4.14
64C	AN25		Alternative: Microcontroller´s P4.11
65C,	AN24		Alternative: Microcontroller´s P4.9
66C,	AN22		Alternative: Microcontroller´s P4.8
68C,	AN19		Alternative: Microcontroller´s P4.6
69C,	AN17		Alternative: Microcontroller´s P4.3
70C;	AN16		Alternative: Microcontroller´s P4.1
71C,	AN14		Alternative: Microcontroller´s P4.0
73C,	AN11		Alternative: Microcontroller´s P0.14
74C	AN9		Alternative: Microcontroller´s P0.11
75C	AN8		Alternative: Microcontroller´s P0.9
76C,	AN6		Alternative: Microcontroller´s P0.8
78C	AN3		Alternative: Microcontroller´s P0.6
79C,	AN1		Alternative: Microcontroller´s P0.3
80C	AN0		Alternative: Microcontroller´s P0.1 Alternative: Microcontroller´s P0.0
62C, 67C, 72C, 77C	AGND	-	Analog Ground 0V for the TC1796 ADC. AGND is connected with GND via R51

Pin Number	Signal	I/O	Description
Pin Row X3D			
1D, 2D	3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D	GND	-	Ground 0 V
4D, 5D, 6D, 7D,	NC P9.5 P4.4 P4.5 P4.6	-	not connected until revision PL2197.1 since revision PL2197.2 X3D-4 is P9.5 X3D-5 is P4.4 X3D-6 is P4.5 X3D-7 is P4.6
8D	NC P4.7	-	not connected pins until PL2197.1 since revision PL2197.2 X3D-8 is P4.7
10D	/RESIN	I	Reset input, controls the system reset /PORST
11D, 12D 13D 15D	 P80 P81 P83 P86	I/O	I/O port P8 Alternative: signals of MSC0 Interface if RN25 is populated **default: RN25 is NOT populated**
16D	RXD0_TTL	I	Receive line of first TC1796 UART Alternative: port P5.0 If the alternative function is used, solder jumper J33 must be open in order to disconnect the RS-232 transceiver from the signal
17D	TXD0_TTL	O	Transmit line of first TC1796 UART. Alternative: port P5.1
18D	CAN_L1	I/O	CANL output of the CAN transceiver for the 2nd TC1796 CAN node Alternative: port 6.10 *(refer to jumper J42)*
20D	CAN_L0	I/O	CANL output of the CAN transceiver for the first TC1796 CAN node Alternative: port 6.8 *(refer to jumper J41)*
21D	CAN_H0	I/O	CANH output of the CAN transceiver for the first TC1796 CAN node. Alternative: port 6.9 *(refer to jumper J41)*
22D	RxD0_RS232	I	RxD input of the RS-232 transceiver for the first serial interface, J33 must be closed to use this interface *(refer to jumper J33)*
23D	TxD0_RS232	O	TxD output of the RS-232 transceiver for the first serial interface J31 must be closed to use this interface *(refer to jumper J31)*
25D	P54	I/O	Microcontroller´s port P5.5
26D	P67	I/O	Microcontroller´s port P6.7 Alternative: Slave select input SLSI1

Pin Number	Signal	I/O	Description
Pin Row X3D			
27D	MRST0	I/O	Master transmit / slave receive output / input of the first synchronous serial interface
28D	MTSR0	I/O	Master receive / slave transmit input / output of the first synchronous serial interface
30D	SCLK0	I/O	Clock input/output of the first synchronous serial interface
31D	SLSI10	I	Slave Select Input of the first synchronous serial interface
32D	SDA0	I/O	Data line of I2C Master controller U11
33D	/IRQRTC	O	RTC interrupt output *Alternative:* ***refer to Appendice A***
35D	E_RX+	I	RxD+ input of the Ethernet Controller U21 *Alternative:* ***refer to Appendice A***
36D	E_TX+	O	TxD+ output of the Ethernet Controller U21 *Alternative:* ***refer to Appendice A***
37D	D+	I/O	USB D+ data line from opt bus-powered USB <-> ASC0 converter (U10)
38D	D-	I/O	USB D- data line from opt bus-powered USB <-> ASC0 converter (U10)
			Microcontroller´s JTAG Interface
40D,	TDI	I	Data Input
41D,	TDO	O	Data output
42D,	TMS	I	State machine control
43D	TCK	I	clock
45D	CAN_H3	I/O	CANH output of the CAN transceiver for the third CAN interface Alternative: Port 6.15, *(refer to jumper J44)*
46D,	P56	I/O	Microcontroller´s port P5.6
			I/O Port 7
47D	P70	I/O	
48D	P72	I/O	Alternative: AD0EMUX0
50D	P75	I/O	
51D	P77	I/O	Alternative: AD1EMUX1

Pin Number	Signal	I/O	Description
Pin Row X3D			
52D, 53D, 55D, 56D, 57D, 58D, 61D, 62D, 63D, 65D, 66D, 67D, 68D, 70D, 71D, 72D, 73D 75D, 76D 77D, 78D	AN43 AN42 AN39 AN37 AN35 AN34 AN29 AN28 AN26 AN23 AN21 AN20 AN18 AN15 AN13 AN12 AN10 AN7 AN5 AN4 AN2	I	Analog Inputs of TC1796 **AN0-AN43 inputs are onboard connected to I/O- ports through RN9-RN18, R29, R30 per default** in order to expose more TC1796 I/O- ports to the phyCORE- connector X3. Alternative: P9.7 Alternative: P9.5 Alternative: P9.3 Alternative: P9.2 Alternative: P4.13 Alternative: P4.12 Alternative: P4.10 Alternative: P4.7 Alternative: P4.5 Alternative: P4.4 Alternative: P4.2 Alternative: P0.15 Alternative: P0.13 Alternative: P0.12 Alternative: P0.10 Alternative: P0.7 Alternative: P0.5 Alternative: P0.4 Alternative: P0.2
60D,	VAREF1	I	TC1796 ADC1 Reference Voltage **R49 connects VAREF1 to 3V3 (default)**
80D	VAREF0	I	TC1796 ADC0 Reference Voltage **R50 connects VAREF1 to 3V3 (default)**
59D, 64D, 69D, 74D, 79D	AGND	-	Analog Ground 0V for the TC1796 ADC. AGND is connected with GND via R51

Table 1: Pinout of the phyCORE-Connector X3

3 Jumpers

For configuration purposes, the phyCORE-TC1796 has 40 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* and indicate the location of the jumpers on the module.

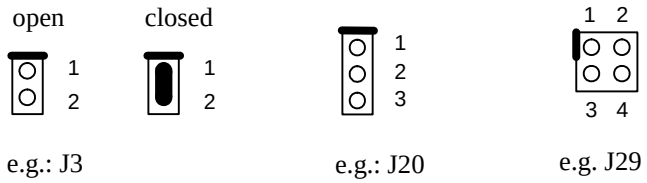

Figure 5: Numbering of the Jumper Pads

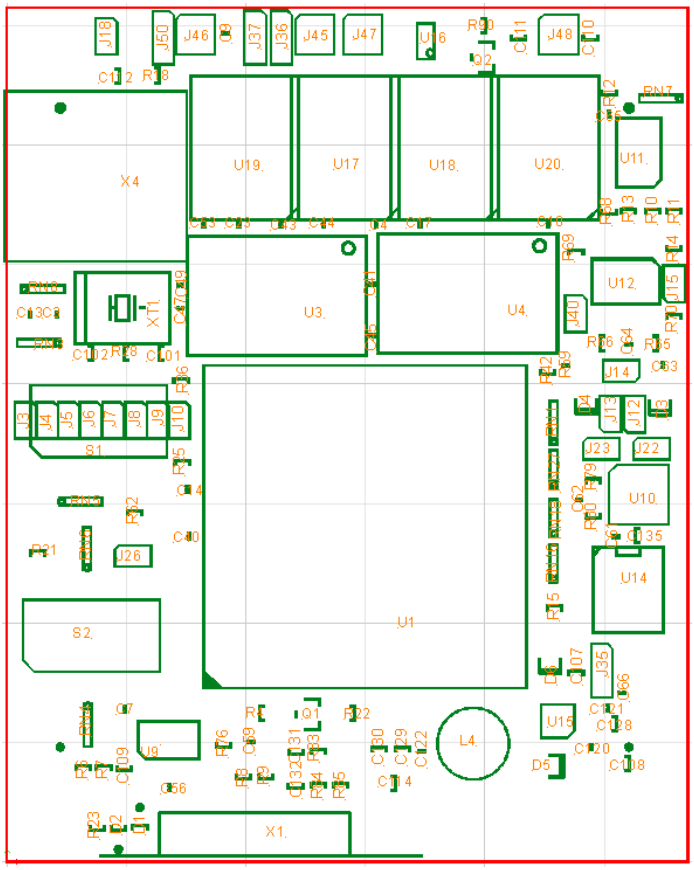

Figure 6: Location of the Jumpers (Controller Side)

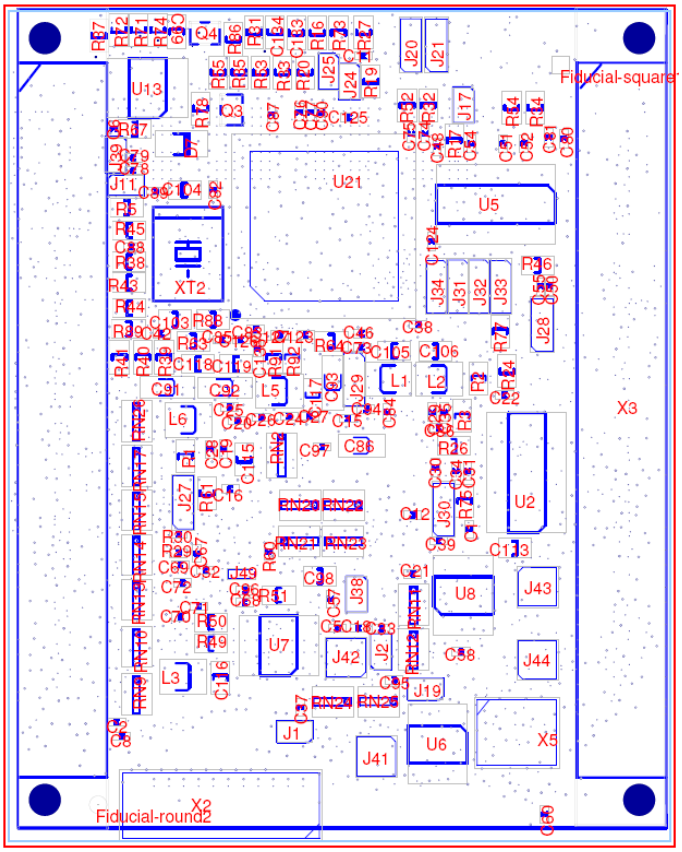

Figure 7: Location of the Jumpers (Connector Side)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Function
J1		**reserved, Do not change !**
open		
closed	**X**	1,5V connected to VDDSBRAM Pin of TC1796
footprint		0R / SMD 0805
J2		**reserved, Do not change !**
open	**X**	
footprint		0R / SMD 0805
J3 – J6		Bootconfig. following a power-on reset (/PORST) If /BOOT = low =>Boot config. Via J[3..6] =HWCFG[0..3] **(access to J3-J6 only available if S1 is NOT populated)**
open	X	Signal is GND
closed		Signal is 3V3
footprint		0R / SMD 0805
J7 – J10		Bootconfig. Following a power-on reset (/PORST) If /BOOT = high =>Boot config. Via J[7..10]=HWCFG[0..3] **(access to J3-J6 only available if S1 is NOT populated)**
open		Signal is GND
closed		Signal is 3V3
footprint		0R / SMD 0805
J11		Connects the MCU´s /CS0 output to the onboard Flash memory U3/U4
open		/CS0 is freely usable on X3
closed	X	/CS0 is connected to the onboard Flash U3/U4
footprint		0R / SMD 0805
J12		Connects the Asynchronous data input (UART RxD) of the optional USB <-> UART bridge U10 with the Microcontroller´s P5.1 (TxD0 ASC0)
open	X	RxD of U10 is NOT connected to Microcontroller´s P5.1 (TxD0 ASC0)
closed		RxD of U10 is connected to Microcontroller´s P5.1 (TxD0 ASC0) **J31 and J33 must be open when J12 is closed**
footprint		0R / SMD 0805

Jumper	Default	Fuonction
J13		Connects the Asynchronous data input (UART TxD) of the optional USB <-> UART converter U10 with the Microcontroller´s P5.0 (RxD0 ASC0)
open	X	TxD of U10 is NOT connected to Microcontroller´s P5.0 (RxD0 ASC0)
closed footprint		TxD of U10 is connected to Microcontroller´s P5.0 (RxD0 ASC0) **J31 and J33 must be open when J13 is closed** 4k7 / SMD 0805
J14		Connects the Tricore SLSO1 alternatively to the phyCORE connector X3C-pin31.
open	X	SCL0 Signal of U11 (I2C_Master I2C_1) is connected To X3C-pin31
closed		Tricore SLSO1 is connected to X3C-pin31 **Caution**: Given that X3C-pin31 is directly connected to SCL0 Signal of U11, **U11 and U14 must NOT be populated when J14 is closed**
footprint		0R / SMD 0805
J15 open footprint J**17**		Connects the MCU´s SLSO2 (SSC Slave Selct Output2) Output to the onboard I2C Master device U12 P2.2 is freely usable on X3 0R / SMD 0805 Connects the MCU´s /CS1 output to the onboard SRAM BANK1 memory U17/U18
open closed footprint	 X	/CS1 is freely usable on X3 /CS1 is connected to the onboard SRAM BANK1 U17/U18 0R / SMD 0805
J**18** open closed footprint	 X	Connects the MCU´s /CS2 output to the onboard SRAM BANK2 memory U19/U20 /CS2 is freely usable on X3 /CS2 is connected to the onboard SRAM BANK2 U19/U20 0R / SMD 0805
J19		Connects the MCU´s P1.15 to control the onboard LED D1
open		P1.15 is NOT connected to control the onboard LED D1
closed	X	P1.15 is connected to control the onboard LED D1
footprint		0R / SMD 0805

J**24**		Connects the MCU´s /CS3 output to the onboard Ethernet Controller U21
open		/CS3 is freely usable on X3
closed	X	/CS3 is connected to the onboard Ethernet Controller U21
footprint		0R / SMD 0805
J25		Connects the MCU´s P1.0 to the onboard IRQ-Output Ethernet Controller U21
open		P1.0 is freely usable on X3
closed	X	P1.0 is input for IRQ of the Ethernet Controller U21
footprint		0R / SMD 0805
J26		Connects P1.14 to microSD card slot for card detect
closed	X	P1.14 connected and used as card detect
open		P1.14 not connected and NOT used as card detect
footprint		0R / SMD 0805

Jumper	Default	Function
J27 open footprint	**X**	**reserved, Do not change !** 0R / SMD 0805
J28 1+2 footprint	**X**	**reserved, Do not change !** 0R / SMD 0805
J29 open closed footprint	**X**	**reserved, Do not change !** 0R / SMD 0805
J30 1+2 2+3 footprint	**X**	**reserved, Do not change !** /HDRST from MCU is peripherals – Reset /PORST from MCU is peripherals – Reset 0R / SMD 0805
J31, J33 1+2, 1+2 2+3, 2+3 footprint	**X**	Roote the signals of the first ASC-Interface (ASC0) Port P5.1 und P5.0 are connected to the RS232 driver U5 Port P6.9 und P6.8 are connected to the RS232 driver U5 **U6 must be unpopulated to use this configuration!** 0R / SMD 0805
J32, J34 1+2, 1+2 2+3, 2+3 footprint	**X**	Roote the signals of the second ASC-Interface (ASC1) Port P5.3 und P5.2 are connected to the RS232 driver U5 Port P6.11 und P6.10 are connected to the RS232 driver U5 **U7 must be unpopulated to use this configuration!** 0R / SMD 0805
J35 1+2 2+3 footprint	**X**	clockout function of the RTC at U14 RTC-Clockout disabled RTC-Clockout enabled 0R / SMD 0805
J36 1+2 2+3, footprint	**X**	This jumper sets the supply for the SRAM BANK1 (U17/U18) depending on the populated memory, Low Power SRAM or High Speed SRAM, on the Module SRAM- BANK1 supply is only 3,3V (for HS-SRAM) SRAM- BANK2 supply is 3,3V or VBAT_IN for LP- SRAM *(refer to section 11 "Standby Power Supply") in this manual* 0R / SMD 0805

Jumper	Default	Function
J37		This jumper sets the supply for the SRAM BANK1 (U19/U20) depending on the populated memory Low Power SRAM or High Speed SRAM on the Module and BANK2
1+2	**X**	SRAM- BANK1 supply is only 3,3V (for HS-SRAM)
2+3,		SRAM- BANK2 supply is 3,3V or VBAT_IN for LP- SRAM *(refer to section 11 "Standby Power Supply") in this manual*
footprint		0R / SMD 0805
J41, J42, J43, J44		These jumpers connect the TTL_CAN signals with the phyCORE connector pins, for connection to external CAN transceivers, or if CAN outputs are used as standard port pins. U6 => CAN Node 0; U7 => CAN Node 1 U8 => CAN Node 2; U9 => CAN Node 3
open	**X**	The on-board CAN transceivers U7, U8, U9, U10 are used.
closed		On-board CAN transceivers must not be populated
1+2/3+4		
Footprint		0R / SMD 0805
J45,J47		These jumpers configure the correct byte control signals being used on the MCU depending on the SRAM devices SRAM BANK1 (U17/U18) populating the module.
1+2/3+4	**X**	low power K6F1616U6C-XF-55 (2 x 2MByte 55ns)
1+3/2+4		high speed CY7C1041DV33-10 (2x 512MByte 10ns)
Footprint		0R / SMD 0805
J46,J48		These jumpers configure the correct byte control signals being used on the MCU depending on the SRAM devices SRAM BANK2 (U19/U20)populating the module.
1+2/3+4		low power K6F1616U6C-XF-55 (2 x 2MByte 55ns)
1+3/2+4	X	high speed CY7C1041DV33-10 (2x 512MByte 10ns)
Footprint		0R / SMD 0805
J49		**reserved, Do not change !**
closed	**X**	
footprint		0R / SMD 0805
J50		Connects speed or transmit Ethernet indication to X3-34C
1+2	**X**	Connect SPD_LED (U21))signal to phyCORE-molex connector X3-34C
2+3		Connect TX_LED (U21) signal to phyCORE-molex connector X3-34C
footprint		0R / SMD 0805

Table 2: Jumper Settings

4 Power System and Reset Behavior

Operation of the phyCORE-TC1796 requires only one supply voltage.

Supply voltage: +3.3 V ± 5 % (max.: 1200mA ; typ.: 400mA)

Once all voltages have reached their target level the voltage supervisory circuit keeps the /PORST reset signal at low level (low is the active level) for additional 200 ms. Then the /PORST signal switches to high level (inactive) and the controller's boot sequence starts.

5 Power-On-Reset Characteristics

When the TC1796 is reset, it needs to know the type of configuration required to start after the reset sequence is finished. The internal state is usually cleared through a reset. This is especially true in the case of a power-up reset. Thus, boot configuration information needs to be applied by the external world through input pins.

Boot configuration information is required for:
• the start location of the code execution
• activation of special modes and conditions

For the start of code execution and activation of special mode, the TC1796 implements two basic booting schemes:
a hardware booting scheme that is invoked through external pins and a software booting scheme in which software can determine the boot options, overriding the externally applied options.

The hardware configuration pins HWCFG[3:0] together with the BRKIN pin, and the TESTMODE choose the boot mode and boot location
(*see System Unit User's Manual for the TC1796, section "Booting Scheme"*).

Start Address following Power-On-Reset
On the phyCORE-TC1796 configuration of two Start addresses after Power-On-Reset is done by using the DIP-switch (S1).
Selection between these two pre-configured start addresses is possible with the help of the /BOOT signal (X3D16):

/BOOT = 1 (inactive)

DIP-switch S1 [4…1]	**HWCFG [3..0]**	**Boot Source**	**PC Start Address**
S1 [4…1] **(default)** [ON,ON,OFF,ON]	0010b	Internal PFLASH memory	A000 0000H

S1 [4…1] [ON,OFF,ON,ON]	0100b	external memory using /CS0	A100 0000H

/BOOT = 0 (active)

DIP-switch S1 [8…5]	**HWCFG [3..0]**	**Boot Source**	**PC Start Address**
S1 [8…5] **(default)** [ON,ON,ON,ON]	0000b (default)	ASC0 Bootstrap Loader	D400 0000H
S1 [8…5] [ON,ON,ON,OFF]	0001b	CAN Bootstrap Loader	D400 0000H

(please refer to System Unit User's Manual section 4.2.7 "Booting Scheme" for additional Bootconfig. for the TC1796)
SWOPT can be configured with the DIP-switchS2 S[8…1]= SWOPT[7…0]with ON=0 /OFF=1)

If "System Start beginning at address A100 0000h" was chosen, then the controller will perform a "blind-read" from address 0x000004 of the memory device attached to /CS0, in order to read the "EBU boot configuration word" (32Bit) (*see section 13.4.3 of the TC1796 Systems Units Manual*). This first read access occurs with the fixed standard values, which support the reading of as many different memory devices as possible. The " EBU boot configuration word " that was read must have valid values for the read access to the memory connected to /CS0, so that the subsequent accesses occur with the correct timing. The values relevant for the timing are subsequently copied to the register BUSCON0. From this point on there is a valid configuration for read accesses to the external Flash memory, and the program execution can begin at address A1000000h.
The valid Boot Configuration Value word for the

phyCORE-TC1796 is 0x0000803D

6 System Memory

In principle, two different memory models are available. The first memory model is the one that is active after a reset. The run time memory model, in contrast, is configured via software by the application.

6.1 Memory Model following Reset

The internal Chip Select logic provided by the TC1796 controller is used exclusively on the phyCORE-TC1796. Hence the memory model as described in the TC1796 User's Manual is valid after reset.

6.2 Runtime Memory Model

The runtime memory model is configured via software using the internal registers of the TC1796. There is a register set containing a BUSCON, BUSAP and ADDSEL register for each of the controllers Chip Select signals. The values in the Bus Configuration Registers (EBU_BUSCON0-3 and EBU_BUSAP0-3) inform the processor of how it should access the connected memory devices (wait states, bus width, etc.). The Address Selection Registers (EBU_ADDSEL0-3) define the address range in which the corresponding Chip Select signal is active. The following list shows the settings for the Chip Select signal assignment.

/CS0 on-board Flash memory or free
/CS1 on-board SRAM bank A or free
/CS2 on-board SRAM bank B or free
/CS3 on-board ethernet controller or free
/CSCOMB free

The runtime memory model is application-dependent. The following table (*Table 3*) shows an example of how such a runtime model can be configured.

Address Range	**Capacity**	**Periphery**	**TC1796 Register**
0xA4000000 0xA4FFFFFF	16MB	on-board Flash (/CS0) or free available	EBU_ADDRSEL0=0xA4000833 EBU_BUSCON0=0x00922200 EBU_BUSAP0=0x80D81D00
0xA0000000 0xA03FFFFF	4 MB	on-board SRAM (/CS1) or free available	EBU_ADDRSEL1=0xA1000853 EBU_BUSCON1=0x00820000 EBU_BUSAP1=0x45B80000
0xA8000000 0xA80FFFFF	1 MB	on-board SRAM (/CS2) or freely available	EBU_ADDR_SEL2=0xA2000873 EBU_BUSCON2=0x00920000 EBU_BUSAP2=0x40D01100
0xD8000000 0xD8007FFF	32KByte	on board ethernet (CS3) or free available	EBU_ADDRSEL3=0xD80000C1 EBU_BUSCON3=0x00420000 EBU_BUSAP3=0x41A00000

Table 3: Runtime Memory Map

EBU_CON = 0x0000FF68

6.3 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-TC1796 provides an easily reprogrammable means of code storage.

The Flash memory operates in 16-bit mode and has 32-bit organization on the module. The phyCORE-TC1796 offers the option of populating up to 64 MByte Flash at U3 and U4. /CS0 is connected to the Flash memory bank. With this configuration this memory bank is active following power-on reset.

6.3.1 Standard Flash

The Intel PC28F640JV3D75 is the standard Flash devices of the phyCORE-TC1796. Depending on the component market situation PHYTEC reserves the right to use other pin-compatible Flash devices from different manufacturers.

These Flash devices are programmable with 3.3 VDC. No dedicated programming voltage is required. Use of Flash memory allows for in-circuit reprogramming of the module.

7 Serial Interfaces

7.1 RS-232 Interface (U5)

One dual-channel RS-232 transceiver is located on the phyCORE-TC1796 at U5. This device converts the signal levels for the RXD0_TTL and TXD0_TTL lines, as well as those of the second serial interface, RXD1_TTL and TXD1_TTL from TTL level to RS-232 level. The RS-232 interface enables connection of the module to a COM port on a host-PC. In this instance the RxD0 line of the transceiver is connected to the TxD line of the COM port; while the TxD0 line is connected to the RxD line of the COM port. The Ground potential of the phyCORE-TC1796 circuitry needs to be connected to the applicable Ground pin on the COM port as well.

The microcontroller's on-chip UART does not support handshake signal communication. However, depending on user needs, hand-shake communication can be software emulated using port pins on the microcontroller. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore there is the possibility of using the TTL signals of the two UART channels externally. These are available on the phyCORE-connector at X3C19, X3C20 (RXD1_TTL, TXD1_TTL) and X3D16, X3D17 (RXD0_TTL, TXD0_TTL). This becomes necessary if galvanic isolation of the interface signals is required.

The TTL transceiver outputs of the on-board RS-232 device can be decoupled from the receive signals RXD0_TTL and RXD1_TTL via solder jumpers J31 and J33. This is necessary so that no external transceivers drive signals against the on-board transceiver. The transmit signals TXD0_TTL / TXD1_TTL, in contrast, can be connected parallel to the transceiver inputs, without causing a collision.

The signals of the two UART are routable CPU internal. This means, that you could choose via configuration register which port Pins are used. Jumper J31, J32, J33, J34 must be set according to your configuration in order to connect the right pins to the RS-232 transceiver.

(refer to Section 3Jumpers and Table2 for settings J31, J32, J33, J34)

7.2 CAN Interface

The phyCORE-TC1796 is designed to house four CAN transceivers at U7, U8, U9 and U10 (SN65HVD23x). The CAN bus transceiver devices support signal conversion of the CAN transmit (CANTx) and receive (CANRx) lines. The CAN transceiver supports up to 120 nodes on a single CAN bus. Data transmission occurs with differential signals between CANH and CANL. A Ground connection between nodes on a CAN bus is not required, yet is recommended to better protect the network from electromagnetic interference (EMI). In order to ensure proper message transmission via the CAN bus, a 120 Ohm termination resistor must be connected to each end of the CAN bus.

Furthermore, it is required that the CANH and CANL input/output voltages do not exceed the limiting values specified for the corresponding CAN transceiver (for the SN65HVD23x -2 VDC / +7 VDC). If the CAN bus system exceeds these limiting values optical isolation of the CAN signals is required.

For larger CAN bus systems, an external opto-coupler should be implemented to galvanically separate the CAN transceiver and the phyCORE-TC1796. This requires purchasing a module without the on-board CAN transceivers installed. Instead, the TxDCANx/RxDCANx signals are routed to the phyCORE-connector with their TTL level. This requires Jumpers closed (*refer to section 3 for details*). For connection of the CANTx and CANRx lines to an external transceiver we recommend using a Hewlett Packard HCPL06xx or a Toshiba TLP113 HCPL06xx fast opto-coupler. Parameters for configuring a proper CAN bus system can be found in the DS102 norms from the CiA[1] (CAN in Automation) User and Manufacturer's Interest Group.

[1]: CiA: CAN in Automation. Founded in March 1992, CiA provides technical, product and marketing information with the aim of fostering Controller Area Network's image and providing a path for future developments of the CAN protocol.

7.3 On-Chip Debug Support (OCDS1)

The TC1796 offers access to its internal OCDS (OCDS = On-Chip Debug Support) module via an expanded JTAG interface. The JTAG interface enables external access to the system without requiring that some sort of service software (i.e. monitor program) run on the target. Standard cross development systems/debug interfaces, such as the GNU TriCore Development Suite from Hightec offer the possibility of setting breakpoints as well as access to the controller's internal registers via the JTAG interface.

The OCDS1/JTAG interface on the TC1796 extends to the phyCORE-connector X3 and a 16-pin (2mm pitch) connector at X1 *(refer to table4 for Pin Assignment)* located on the edge of the phyCORE module. An external converter (Wiggler, etc.) can be connected at X1, which allows for connectivity of the TC1796 to a host PC.
It is then possible to transfer program code to the module and debug this code with the help of standard debug functions such as breakpoints, single step, etc.
Pin1 of the JTAG connector (X1) is marked by an arrow in Figure8.

The phyCORE-TriCORE Develoment Board (order number KSP-0150-B0) integrates such a converter, thus allowing direct connectivity with a development computer (refer to phyCORE-TriCORE Develoment Board HW-Manual).

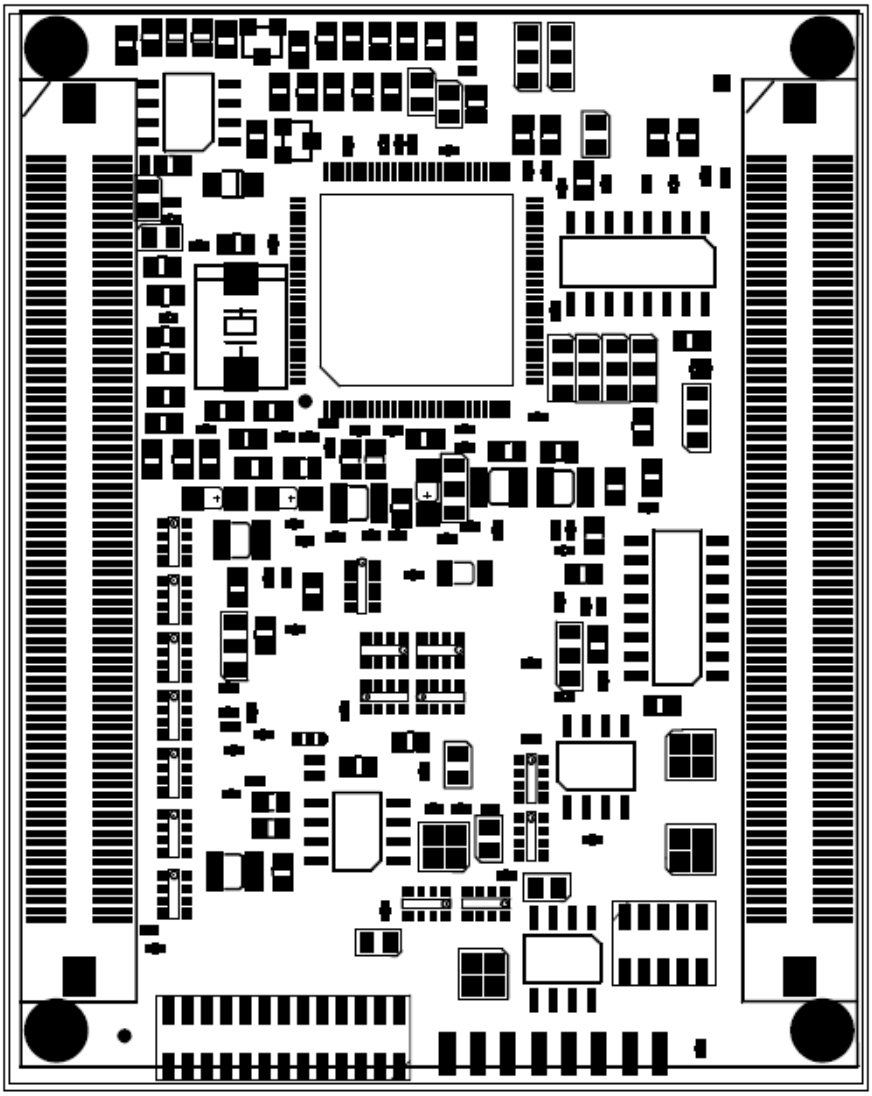

Figure 8: OCDS1/JTAG interface X1 (connector side)

Signal	phyCORE-connector X3	X1	Description
TMS	42D	1	JTAG module state machine control input
3V3	1C	2	Supply voltage for external wiggler
TDO	41D	3	JTAG module serial data output
GND	44D	4	Ground
GND	37C	6	Ground
TDI	40D	7	JTAG module serial data input
/PORST	11C	8	Power-on reset input
/TRST	41C	9	JTAG module reset/enable input
/BRKOUT	40C	10	OCDS break output
TCK	43D	11	JTAG module clock input
GND	39D	12	Ground
/BRKIN	39C	13	OCDS break input
nc.		14	not connected
nc		15	not connected
nc		16	not connected

Table 4: OCDS1 Connector X1 Pin Assignment

7.4 USB to UART Bridge (U10)

One USB to UART Bridge CP2102 is located on the phyCORE-TC1796 at U10.
The CP2102 is a highly-integrated USB-to-UART Bridge Controller providing a solution to transmit and receive UART signals over USB from a Host PC. A Royalty-free Virtual COM Port (VCP) device drivers provided by the chip- manufacturer allow a CP2102-based product to appear as a COM port to PC applications.

5V Supply voltage from USB VBUS must be applied on phyCORE-connector X3C30 because the CP2102 bus-powered on the phyCORE-TC1796.

The TC1796 ASC0 can be connected to communicate over USB to a Host PC. This is done by closing jumper J12 and J13 **(open per default)** so that RxD0 (P5.0) of the TC1796 is connected to the UART Transmit of CP2102 and TxD0 (P5.1) of the TC1796 is connected to the (UART Receive).

Please refer to jumper J12 and jumper J13 in section 3

Furthermore it is possible to activate the /Boot and /PORST by using the R232 handshake Output Signals RTS (Request to Send) and DTR (Data Terminal Ready) provided by the CP2102.

RTS can control the /Boot signal (used for alternative Bootmode)
DTS can control the /PORST signal (system Reset)

In order to use this feature the optional resistors J22 an J23 must be populated with 0R (unpopulated per default)

Caution:
USB to UART Bridge is NOT connected to the TxD0 and RxD0 in the standard phyCORE TC1796 module configuration.

8 Hardwired TCP/IP Ethernet Controller (U21)

The phyCORE-TC1796 is equipped with a Ethernet Controller W5300. The W5300 is a single chip into which 10/100 Ethernet controller, MAC, and TCP/IP are integrated.
The Ethernet Controller operates in 16-bit mode and is connected to /CS3 of the Microcontroller's External Bus Interface.
The Signals LINKLED (U21) is routet to X3-33C and can be connected to an LED to indicate the link status of media(10/100M).
The Signals SPD_LED is or TXLED (Transmit Act LED) can be routet to X3-34Cconfigured by jumper J50.
(Refer to jumper J50 in section 3)

On the phyCORE-TC1796 the Ethernet controller W5300 is implemented to operate in direct address mode and internal PHY mode.
Please refer to the datasheets of the W5300 for information, how to initialize and program the Ethernet-interface.
Also refer to the datasheets of the W5300 for the needed Transformer characteristics.

8.1 MAC Address

In a computer network such as a "local area network" (LAN), the MAC (Media Access Control) address is a ***unique*** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.
In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-TC1796 is located on the bar code sticker attached to the module.
This number is a 12-position HEX value. The MAC address has already been programmed into the serial SPI-EEPROM and should be used by your application. The location of the MAC address in the SPI-EEPROM is from 0x00 to 0x0B. Where the most significant byte is at address 0x00 and the least significant byte is at 0x0B.

The following example shows the address and its content of a stored MAC address in the SPI-EEPROM:
Every position of the MAC address is stored as a binary value in the SPI – EEPROM

MAC address Example 0050C2A0C093

SPI-EEPROM address	Stored Byte
0x00	00
0x01	00
0x02	05
0x03	00
0x04	0C
0x05	02
0x06	0A
0x07	00
0x08	0C
0x09	00
0x0A	09
0x0B	03

9 SPI to IIC Master Controller SC18IS600 (U11 / U12)

The phyCORE-TC1796 features two onboard SPI to IIC-BUS Master
Controller SC18IS600. The SC18IS600 acts as a bridge between a SPI interface and an I2C-bus. It allows a SPI master device to communicate with I2C-bus slave devices.

The IIC interface controller supports a certain protocol to allow devices to communicate directly with each other via two wires. One line is responsible for clock transfer and synchronization (SCL), the other is responsible for the data transfer (SDA).
The IIC Bus Controller SC18IS600 provides communication at data rates of up to 400 kbit/s and controls all the I2C-bus specific sequences, protocol, arbitration and timing.

Because the phyCORE-TC1796 has populated two of IIC-BUS Master Controller, it provides the Signals for two independent IIC-Buses on the phyCORE-connector at X3C31, X3D32 (SCL0, SDA0) and X3C25, X3C24 (SCL1, SDA1)

The two IIC-BUS Master Controller on the phyCORE-TC1796 are both controlled by the Microcontroller's SSC0 interface.
The slave select for the first (U11) IIC Interface controller (SCL0, SDA0) is SLSO1 (SSC Slave Select Output 1) and the slave select for the second (U12) IIC Interface controller (SCL1, SDA1) is SLSO2 (SSC Slave Select Output 2) (P2.2)

If you want to connect more than one I²C devices externally to a IIC Interface, each device is to be assigned a unique address to avoid collisions when addressing the devices. Furthermore make sure that the baud rate used for data transfer is adjusted to the slowest device.
Please refer to the datasheets of the SC18IS600 for information, how to initialize and program the IIC BUS- Master Controller.

10 SPI Memory, EEPROM / FLASH (U13)

The phyCORE-TC1796 features a non-volatile memory with an SPI interface. This memory can be used for storage of configuration data or operating parameters, that must not be lost in the event of a power interruption. Depending on the module's configuration, this memory can be in the form of an EEPROM (per default) or FLASH with the available capacity from max. 32 kByte for EEPROM and
max. 2MByte for Flash memory

The memory is connected to the Microcontroller’s SSC0 interface. Using SLSO0 (SSC Slave Select Output 0) for enabling the memory

11 Real-Time Clock RTC-8564 (U14)

For real-time or time-driven applications, the phyCORE-TC1796 is equipped with an RTC-8564 Real-Time Clock at U14. This RTC device provides the following features:

- Serial input/output bus (I^2C), address 0xA2
- Power consumption
  Bus active (400 kHz): < 1 mA
  Bus inactive, CLKOUT inactive: < 1 µA
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

If the phyCORE-TC1796 is supplied with a +3VDC voltage at Pin X3C6C (VBAT_IN), the Real-Time Clock runs independently of the board's power supply.

Programming the Real-Time Clock is done via the first IIC (U11) Interface controller (SCL0, SDA0).
The I2C Slave address of RTC-8564 is 0xA2/0xA3.

The Real-Time Clock also provides an interrupt output that extends to the phyCORE connector X3D33D. An interrupt occurs in case of a clock alarm, timer alarm, timer overflow and event counter alarm. An interrupt must be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications. *For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.*

Note:
After connection of the supply voltage, or after a reset, the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*)

12 Standby Power Supply

In some applications it is desirable to disconnect all supply voltages from the module, but still maintain certain data in the volatile memory. For such cases the phyCORE-TC1796 offers the input pin VBAT_IN (X3C6).
If a voltage of 3.1 V is supplied over VBAT, then the data is maintained in the RTC and depending on the Hardware configuration in the SRAM memory device mounted at BANK1 U17/U18 or BANK2 U19 /U20 (*refer jumper J36 and J37*), even if all other supply voltages have been turned off.
Connecting a battery via the VBAT_IN input is not mandatory for normal operation of the module, since all devices listed above are supplied with power by the module's operating voltage 3V3.

13 OCDS2 debugging

The phyCORE-TC1796 provides the OCDS2 Trace signals at connector X2. This connector is not the standard OCDS2 interface. It enables only the possibility to route the OCDS2 Trace signals to the carrier Board for the phyCORE-TC1796 such as the phyCORE-TriCORE Development Board. On the carrier board then, the Trace Signals are routed to the standard 60 Pin Highspeed connector for OCDS2 debugging.
This is done on the TriCORE Development Board for the phyCORE-TC1796

Please contact PHYTEC for information regarding the mate connector of the OCDS2 connector X2 on the phyCORE-TC1796

14 microSD-card slot X4

The phyCORE-TC1796 features a microSD Card slot.
The microSD is connected to the Microcontroller's SSC1 interface.
using SLSO7 (SSC Slave Select Output 7) for the microSD

Furthermore Port Pin input P1.14 is used to as card detect input.
If a microSD is inserted (P1.14 is low) or not inserted (P1.14 is high)
This feature can be enabled disabled by setting jumper 26
refer jumper J26 in section 3

15 Technical Specifications

The physical dimensions of the phyCORE-TC1796 are represented in *Figure 9*. The module's profile is ca. 7 mm thick, with a maximum component height of 2 mm on the backside of the PCB and approximately 3 mm on the top side. The board itself is approximately 2 mm thick.

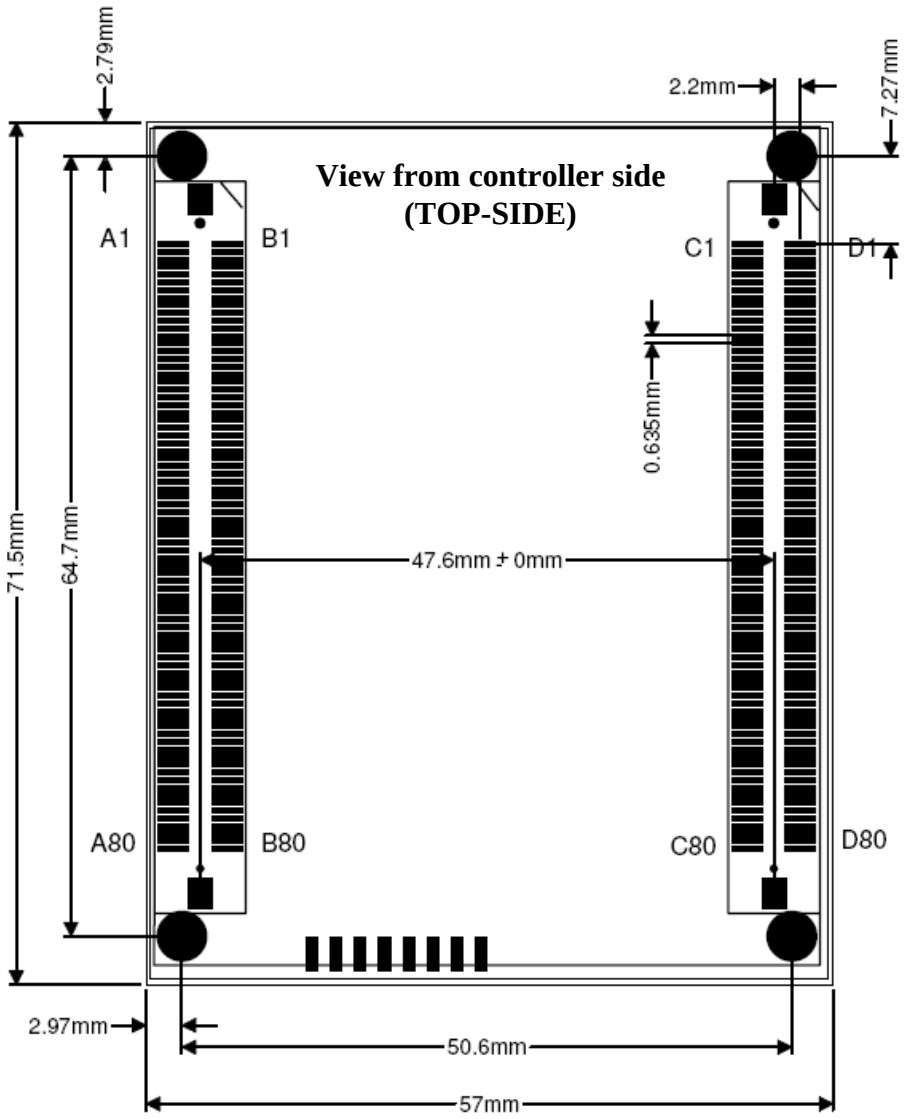

Figure 9: *Physical Dimensions TOP VIEW*

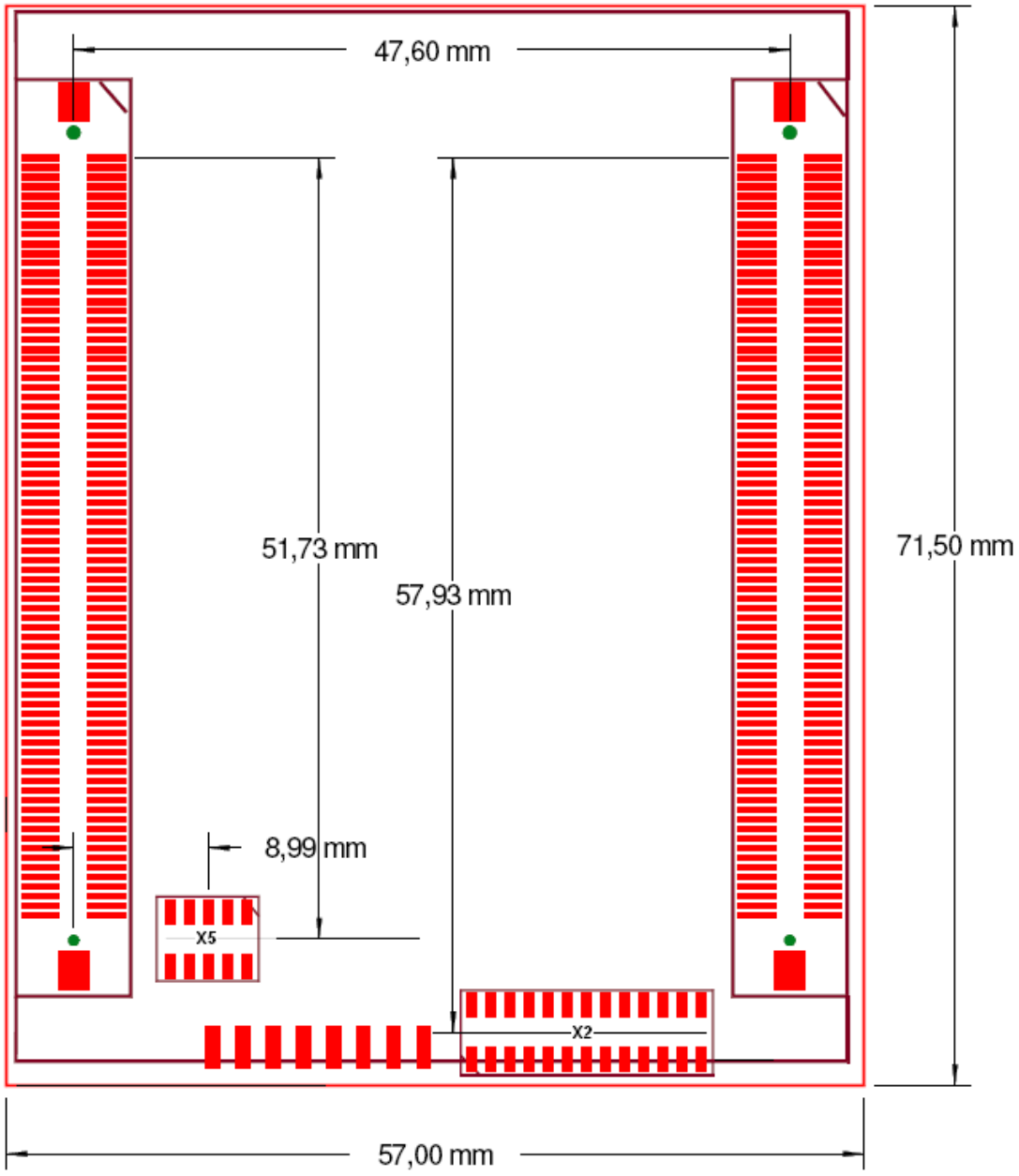

Figure 10: X5 and X2 *Dimensions TOP VIEW*

technical specifications:

• Dimensions:	71,5 mm x 57 mm
• Weight:	approximately 26 g with all optional components mounted on the circuit board
• Storage temperature:	-55°C to +125°C
• Operating temperature:	standard: -40°C to +85°C except ethernet W5300 0°C to +80°C
• Humidity:	95 % r.F. not condensed
• Operating voltages:	3.3 V ±5 % VBAT 3 V ±5 %
• Power consumption:	Conditions: 150 MHz clock, 4 MByte LP-RAM,
3.3 V voltage	1 MByte HS-RAM, 32MByte Flash, 20°C max. 1200mA typ. <400 mA
Battery current draw Real-Time Clock supply	Conditions: VBAT = 3 V 3.3 V voltage=off, 20°C 270nA

These specifications describe the standard configuration of the phyCORE-TC11796 as of the printing of this manual

Connectors on the phyCORE-TC1796:

Manufacturer	Molex
Number of pins per connector row	160 (2 rows of 80 pins each)
Molex type number	52760 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-TC1796. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2 mm) on the underside of the phyCORE must be subtracted.

- Height 6 mm

Manufacturer	Molex
Number of pins per connector row	160 (2 rows of 80 pins each)
Molex type number	55091 (plug)

- Height 10 mm

Manufacturer	Molex
Number of pins per connector row	160 (2 rows of 80 pins each)
Molex type number	53553 (plug)

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

16 Hints for Handling the phyCORE-TC1796

Removal of components is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Integrating the phyCORE-TC1796 in application circuitry

Successful integration in user target circuitry depends on whether the layout for the GND connections matches those of the phyCORE module. It is recommended that the target application circuitry is equipped with one layer dedicated to carry the GND potential. In any case, be sure to connect all GND pins neighboring signals which are used in the application circuitry. For the supply voltage, there must be contact with at least six of the GND pins neighboring the supply voltage pins.

17 Revision History

Date	Version numbers	Changes in this manual
22 October-2008	Manual L-719e_0 KSP-0150-0 PCB# PL2197.0	Preliminary edition.
12. March - 2009	Manual L-719e_1 KSP-0150-1 PCB# PL2197.1	1st edition.
29.May - 2009	Manual L-719e_2 KSP-0150-1 PCB# PL2197.1	2nd edition. - change: J18 open per default - correction on page19 CAN_H0 is Port 6.9 - MAC address stored in SPI-EEPROM added on Page 42, 43 - correction: table1 page 16 Alternative function of X3C-13, X3C-14, X3C-15, X3C-16 is MSC1 - correction: table1 page 19 Alternative function of X3D-11, X3D-12, X3D-13, X3D-15 is MSC0
24.Sept – 2010	Manual L-719e_3 KSP-0150-1 PCB# PL2197.2	3rd edition. - modified: table1 page 19 Alternative function of X3D-11, X3D-12, X3D-13, X3D-15 is MSC0 if RN25 is populated - modified: page 52 Operating temperature: standard: -40°C to +85°C - added description of J14 page 25 - Figure 10: X5 and X2 Dimensions added page 51 - changes on page 16 X3C-4 is P9.4 X3C-5 is P5.7 - changes on page 20 X3D-4 is P9.5 X3D-5 is P4.4 X3D-6 is P4.5 X3D-7 is P4.6 X3D-8 is P4.7 - modified: table1 page 17 X3C-38 TRCLK Trace Clock for OCDS Level 2 - description of optional RN26 and RN27 in chapter "A.1 Release Notes " page56 - change in pages 18/21: AN0-AN43 are onboard connected to I/O- ports through RN9-RN18, R29, R30 default - modified description of RESOUT on page 16

Appendice A

A.1 Release Notes

The following paragraph describes the differences between the technical facts provided in this manual and the currently available hardware revisions.

phyCORE-TC1796 modules with PCB number PL2197.1 that were delivered before the 29. May 2009 have the configuration J18=closed.

With the pcb revision 2197.2 it is possible to connect the Port 9.0 to 9.7 Signals directly to the phyCORE -Connector X3 by populating the resistor networks RN26 and RN27.
Populating RN26 and RN27 is only possible if U21 (Ethernet) and U14 (RTC) is NOT populated. Thus no Ethernet and I2C_1 Master controller are available in this configuration.
Caution: This is not the default configuration of the phyCORE-TC1796 module. Thus RN26 and RN27 are NOT populated in the standard phyCORE-TC1796 configuration.

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Document: **phyCORE-TC1796**
Document number: **L-719e_3, Sept. 2010**

How would you improve this manual?

Did you find any mistakes in this manual? page

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