Implemented workaround on the phyFLEX-i.MX 6 SOM (PFL-A-02) related to random boot failures of the controller

The information in this document is relevant for deployment of the phyFLEX-i.MX 6 System on Module with root part # PFL-A-02, as well as corresponding Rapid Development Kits with root part # KPFL-A-02 which are populated with Freescale i.MX 6 controllers prior to silicon revision 1.2.2.

Freescale's i.MX 6 controllers show a random boot failure which is described in **Errata ERR006282** – "**ROM code uses nonreset PFDs to generate clocks, which may lead to random boot failures"** from Freescale. This failure is only relevant for boot configurations using the NAND, or the SD/MM card (Boot Mode 0 and 3 on the phyFLEX-i.MX 6).

Workaround implemented:

A watchdog function implemented in the Control Management IC (CMIC) at U17 on the phyFLEX-i.MX 6 (PCB 1362.2 et seqq.) prevents the system to hang in an unknown state (refer to workaround #3 described in the Errata). This means that the CMIC generates a reset of the controller, if the boot sequence does not complete within a certain time. In order to allow the correct and complete execution of the boot sequence the time-out period is different for each boot mode. Thus the configured watchdog time ensures that all boot sources will be searched for an image within the time-out period.

Table 1 shows the time-out period for the different boot modes.

Boot mode	Description	Watchdog time
0	NAND boot	6 s.
3	SD card boot	15 s.

Table 1: Time-out Periods for different Boot Modes

Translation into software code:

Six easy steps is all that is need to implement the workaround in the barebox.

1. Configure pin A20 (SD4_DAT3/GPIO2_IO11) as output and initialize it to '1'
2. Verify the correct initialization and provide an error message in case of failure
3. Wait 20 ms to ensure the detection of the high level by the CMIC
4. Set the output to '0'. This results in the desired falling edge at the CMIC_WAKE input of the CMIC which indicates the complete execution of the boot sequence
5. Deactivate the pull-up at the output
6. Change the signal direction of pin A20 (SD4_DAT3/GPIO2_IO11) to input in order to allow use of this pin as WAKE-UP input.

This procedure should be implemented right after the muxing.

The following extract shows the implementation in the BSP (PD13.2.0 et seqq.) delivered with the module:

```
#define MX6_PHYFLEX_ERR006282   IMX_GPIO_NR(2, 11)
  /*MX6_PHYFLEX_ERR006282 represents the CMIC_WAKE signal*/

static void phyflex_err006282_workaround(void)
{
  if (gpio_direction_output(MX6_PHYFLEX_ERR006282, 1) != 0)
    printf("gpio_direction_output(MX6_PHYFLEX_ERR006282,  0)
            failed\n");

  mdelay(20);
  gpio_set_value(MX6_PHYFLEX_ERR006282, 0);
  mxc_iomux_v3_setup_pad(MX6Q_PAD_SD4_DAT3__GPIO_2_11_PD);
  gpio_direction_input(MX6_PHYFLEX_ERR006282);
}
```

The source file including this sequence (board.c) can be found in arch/arm/boards/phytec-pfla02/.

Note:
It is mandatory to toggle the CMIC_WAKE signal in any case to ensure the correct functioning of the CMIC's wake up mechanism.

Please contact our support if you need any further information.

Germany and Europe (except France):	France:
▪ +49 (6131) 9221-31	▪ +33 (0) 2 43 29 22 33
▪ support@phytec.de	▪ support@phytec.fr
North America:	India:
▪ +1 (206) 780-9047, or +1 (800) 278-9913	▪ +91 (80) 4130-7589
▪ support@phytec.com	▪ support@phytec.in