Using 28F128J3D Flash on the phyCORE-MCF548x

Application Note

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Preface

This Application Note describes how to use Intel® 28F128J3D Embedded Flash memory populating the phyCORE-MCF548x.

Initial phyCORE-MCF548x modules were populated with 28F128K3 Intel Strata Flash devices. Due to changes with the Intel Flash µBGA packaging PHYTEC switched to the 28F128J3D Embedded Flash memory on new production runs.

For general startup instructions of your phyCORE-MCF548x (PCM-024) please refer to the phyCORE-MCF548x Hardware Manual L-645. Precise specifications for Freescale's ColdFire MCF548x controller can be found in the corresponding Data Sheet/User's Manual.

1 ColdFire MCF548x Register Settings for 28F128J3D Flash

The Flash memory is connected to the ColdFire's FlexBus controlled by Chip Select 0 (/FB_CS0).

The chip select is configured by the registers

Chip Select Address Register	CSAR0	(offset 0x0500)
Chip Select Mask Register	CSMR0	(offset 0x0504)
Chip Select Control Register	CSCR0	(offset 0x0508)

These registers are accessible relative to the base address configured in the MBAR register.

Module Base Address Register	MBAR	(offset 0x0c0f)

MBAR resides in CPU supervisor space and is accessible with the MOVEC opcode.

```
/* Initialize MBAR to 0x10000000*/
move.l  #10000000h,D0
movec     D0,MBAR
```

For this example the registers CSAR0, CSMR0 and CSCR0 are accessible on addresses 0x10000500 to 0x10000508.

1.1 Chip Select Address Register (CSAR0)

CSAR0 configures the base address for /FB_CS0. After Reset the base address is pre-initialized to address 0x00000000 and the Flash memory is accessible in the whole address range of the processor.

Name	Bit(s)	Value (hex)	Description
BA	[31..16]	default 0x0000	Base address for the Flash memory. BA is compared with the upper internal address bus A[31..16]. Default after Reset is base address 0x00000000. Normally the base address is changed to 0xFC000000 for runtime due to the DDR SDRAM is mapped to base address 0x00000000.
reserved	[15:0]	0x0000	-

Recommended for runtime:
CSAR0 = 0xFC000000 // Base address 0xFC000000

1.2 Chip Select Mask Register (CSMR0)

CSMR0 configures the space of /FB_CS0. Amount of space must be at minimum as large as the Flash memory devices provide.

Name	Bit(s)	Value (hex)	Description
BAM	[31..16]	default 0x0	Address Mask. Setting a BAM bit causes the corresponding address bit to be a "don't care". The block size is 2^n with n = (number of bits set in BAM+16). 16MByte BAM=0x00FF 32MByte BAM=0x01FF 64MByte BAM=0x03FF After Reset, /FB_CS0 acts as global chip select and is active in for the whole address range.
reserved	[15:9]	0x0	-
WP	[8]	default 0	Write Protection disabled
reserved	[7..1]	0x0	-
V	[0]	default 0	Valid bit. Setting this bit indicates whether the corresponding CSAR, CSMR and CSCR contents are valid.

Recommended for runtime:
CSMR0 = 0x03FF0001 // 64MBye space

1.3 Chip Select Control Register (CSCR0)

CSCR0 configures the timing characteristics of the Chip Select /FB_CS0.

Name	Bit(s)	Value (b)	Description
SWS	[31..26]	000000	Secondary wait states
reserved	[25:24]	00	-
SWSEN	[23]	0	Secondary wait state disabled
reserved	[22]	0	-
ASET	[21..20]	01	1 cycle address setup
RDAH	[19..18]	0	Read address hold
WRAH	[17..16]	010	Wite address hold
WS	[15..10]	000100	4 Wait states for 28F128J3D
reserved	[9]	0	-
AA	[8]	1	Internal /TA generation depending on WS
PS	[7..6]	00	32-bit Port Size
BEM	[5]	0	Byte Write Enable mode
BSTR	[4]	0	Burst read disabled
BSTW	[3]	0	Burst write disabled
reserved	[2..0]	000	-

Recommended for runtime:
CSCR0 =0x00101100 // 1 Address-Setup cycle and 4 Wait states

1.4 Register Programming Order

The CSMR0 should be the last register, because of programming the V bit to 1 activates the Chip Select.

Example:
CSAR0 = 0xFC000000 // Base address to 0xFC000000
CSCR0 = 0x00101100 // 1 Address-Setup cycle and 4 Wait states
CSMR0 = 0x03FF0001 // 64MByte space and V=1 for activation