

Use of new NOR Flash Parts on phyCORE-MPC5200B-tiny and phyCORE-MPC5200B-I/O (PCM-030 and PCM-032)

The information in this document is important and must be followed if you are using phyCORE-MPC5200B-tiny, or phyCORE-MPC5200B-I/O SOMs with order code PCM-030-x1xxxxxxx, or PCM-032-x1xxxxxxx, or corresponding kits (KPCM-...).

Introduction

The NOR Flash parts used on the original design of the PHYTEC phyCORE-MPC5200 System-on-Modules were supplied by Intel under the name P33 Strata Flash®. Later, production rights were transferred to Numonyx and subsequently to Micron. The NOR Flash product name also changed to P33 Axcell™ Flash.

In addition Numonyx changed the production process for these components by performing a "die shrink" to a state-of-the-art 65nm process. Besides a number of changes to the component characteristics and values as depicted in the data sheet there are also new erratas that apply to the current A1 step product revision which need to be taken into consideration

This applies to the following Flash type:

PC28F256P33xF

One of the most significant changes is the 10 ns longer access time. Besides the changes in access timing our component validation investigation found that the new erratas that have been released for this modified Flash part need to be considered. PHYTEC's research has also shown that the errata called "Flexlock Write Timing" can occur and therefore it is strongly recommended that customers implement the work-around suggested by the component manufacturer Micron.

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Micron plans to release a new P33 Flash revision (A2 step) which will fix this errata. Unfortunately market release of this new A2 step has been delayed which forces PHYTEC to use the current A1 step component with all its known erratas and the resulting possible impact on customer applications in order to continue to deliver phyCORE-MPC5200 SOMs.

The following sections will address the currently known changes identified by PHYTEC and their potential impact on the overall system behavior in conjunction with the phyCORE-MPC5200.

Impact of NOR Flash Change on phyCORE-MPC5200B-tiny and phyCORE-MPC5200B-I/O

1. Verification of configured timing values

PHYTEC's Linux BSP uses a configuration with 33 MHz PCI clock, which is also the basis for Flash access timing along with 2 wait states for NOR Flash access. This represents the fastest possible access configuration for both the originally used Intel Strata Flash parts and the newer Micron Axcell™ Flash. As a result no timing modifications are necessary as a result of this part change.

However, when using a different configuration (such as 66 MHz PCI clock) it is possible to set up timing values that may be allowed for operation with the Intel Strata Flash but not the Micron Axcell™ Flash parts. In this case it will become necessary to verify the configured timing to ensure proper operation in conjunction with the new Micron Axcell™ Flash parts and make changes if needed.

2. Implementing the work-around for A1 step errata "Flexlock Write Timing"

During validation of phyCORE-MPC5200 SOMs populated with Micron Axcell™ Flash parts within a UBoot/Linux environment the behavior reported in the errata note could not be observed. However, it is conceivable that the symptoms described in the errata may occur using a different software/hardware environment. It is therefore recommended to implement the work-around in your software as a precautionary measure.

Sample source code for implementing this work around in your software is available on our FTP server.

PCM-030 Linux:

<ftp://ftp.phytec.de/pub/Products/phyCORE-MPC5200/pcm030/OSELAS-6/IM590/>

PCM-030 WinCE:

<ftp://ftp.phytec.de/pub/Products/phyCORE-MPC5200/pcm030/wince/IM590/>

PCM-032 Linux:

<ftp://ftp.phytec.de/pub/Products/phyCORE-MPC5200/pcm032/Linux/IM590/>

PCM-032 WinCE:

<ftp://ftp.phytec.de/pub/Products/phyCORE-MPC5200/pcm032/Linux/IM590/>

Summary and Additional Resources

The information in this document has been compiled by PHYTEC to the best of our knowledge. In addition we recommend checking additional documents provided by Micron/Numonyx related to this Flash part revision.

Furthermore it is strongly recommended to perform in-system validation tests using the specific hardware and software environment of your end application.

A complete library of related P33 NOR Flash datasheets, application and errata notes is available on the following URL (as of the time of creating this TechNote):

<http://numonyx.com/en-US/MemoryProducts/NOR/Pages/P30P33Documents.aspx>

References

Conversion Guide: Numonyx® Axcell™ Flash Memory P33 Stack 256-Mbit/256-Mbit (130nm) to 512-Mbit monolithic (65nm)
Application Note - 309015
Apr 2010

Numonyx® Axcell™ Flash Memory (P33-65nm)
256-Mbit, 512-Mbit (256M/256M)
Datasheet, Order Number: 320003-09
Mar 2010